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UPDATED FILING RECEIPT

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REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
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Date Mailed: 03/26/2002

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Assignment For Published Patent Application

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Mitsubishi Silicon America Corporation;

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Title

Linearity measuring apparatus for wafer orientation flat

Preliminary Class

073

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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EXHIBIT 7

Subject: MSA01001の訂正原稿
Date: Fri, 25 May 2001 08:59:26 +0900
From: Masayoshi Suda <suda@tm.kcom.ne.jp>
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MSA01001C.doc	Name: MSA01001C.doc Type: Microsoft Word Document (application/msword) Encoding: base64
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fig8.TIF	Name: fig8.TIF Type: TIFF Image (image/tiff) Encoding: base64

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Dear Mr. Nobuyuki Hayashi,

I reviewed and revised the patent draft description [redacted]

I attach hereto my revised version of the [redacted]

Also, please let me know the [redacted]

I would like to see the actual tool so that you can [redacted]

Masayoshi Suda, Patent Attorney in Tokyo

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LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a measuring apparatus [redacted] the linearity of an orientation flat (hereinafter referred to as an Ori-Fla).

Description of Related Art

Conventionally, [redacted]

On the other hand, there has been disclosed a wafer Ori-Fla positioning method in which an Ori-Fla is positioned by pressing a wafer against a positioning mechanism provided on a wafer chuck mounting surface (Unexamined Japanese Patent Publication No. 10-22368). In this positioning method, the wafer chuck mounting surface is provided so as to be inclined, and a gas flow for floating a wafer with respect to a wafer chuck is generated by air blowing means.

In the positioning method configured as described above, when air is blown from the air blowing means in a state in which a wafer is mounted on the wafer chuck mounting surface, the wafer moves smoothly under gravity toward a positioning mechanism along the inclination of the wafer chuck mounting surface. As a result, the positioning of the Ori-Fla can be performed reliably.

Further, there has been disclosed an exposure device

that has a stage, a rough positioning mechanism, and number detecting means, and can perform exact rough positioning of a wafer without pattern at the time of first-level pattern exposure (Unexamined Japanese Patent Publication No. 8-78316). In this exposure device, at least three stopper members are provided to roughly position a wafer on the stage, and the stage moves in the longitudinal and transverse X & Y directions and in the rotation direction of θ. Also, the rough positioning mechanism performs rough positioning by causing the peripheral portions of wafer mounted on the stage to abut against the stopper members. Further, the number detecting means detects an identification number scribed on the wafer positioned roughly so that the wafer moves on the stage until the identification number arrives at a predetermined position.

In the conventional method in which the linearity of the Ori-Fla portion is examined visually, however, the acceptability or non-acceptability of linearity cannot be determined quantitatively. Also, in the conventional Ori-Fla positioning method disclosed in the aforementioned Unexamined Japanese Patent Publication No. 10-22368, or in the exposure device disclosed in Unexamined Japanese Patent Publication No. 8-78316, the fabrication accuracy of the Ori-Fla, especially the fabrication accuracy in chamfering the Ori-Fla is poor because the linearity of the Ori-Fla of wafer itself is not measured. For example, when as shown in FIG. 8(a), a vertex P is formed at the center of an Ori-

Fla 8a, and the Ori-Fla 8a is formed of a first side 8b and a second side 8c on opposite sides of the vertex P, there arises a problem in that the crystalline orientation of a wafer 8 deflects comparing the time when the first side 8b is aligned with the positioning mechanism with the time when the second side 8c is aligned with the positioning mechanism. Further, the Ori-Fla 8a of the wafer 8 as shown in FIG. 8(b) also presents the same problem. [redacted]

SUMMARY OF THE INVENTION

[redacted]

[redacted]present invention provides a linearity measuring apparatus for a wafer orientation flat, comprising a base in which [redacted] straight tracks are formed in a first direction; a platform which is configured so as to be movable in the first direction by being engaged with the straight track via engagement means, and is further provided with a top surface formed so as to be flat to

mount a wafer having an orientation flat; a block which is installed on the base with a predetermined first clearance L being provided with the straight track in a second direction perpendicular to the first direction, and has a flat face against which the orientation flat of the wafer mounted on the platform abuts and which is parallel with the first direction; wafer fixing means provided in the platform to fix the wafer in a state in which the wafer is mounted on the platform; and a [redacted] which is installed on the base with a predetermined [redacted] clearance M being provided with the block in the first direction, and has a probe opposed to the straight track and capable of being displaced in the second direction, wherein when the clearance between the tip end of the probe and the straight track is taken as N, the following equation (1) is satisfied

[redacted] .....

In order to measure the linearity of an Ori-Fla by using the linearity measuring apparatus for a wafer Ori-Fla in accordance with the present invention, the platform on which a wafer is not mounted is first moved in the first direction so as to be opposed to the block. Next, a wafer is mounted on the top surface of the platform, and the Ori-Fla of the wafer is allowed to abut against the flat face of block so that the Ori-Fla is substantially parallel with the flat face. Thereafter, the wafer is fixed on the platform by the wafer fixing means. Next, the platform is

moved in the first direction, by which the Ori-Fla is brought into [redacted] with the probe of the [redacted]. Further, the platform is moved in the first direction, by which the probe of the [redacted]

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of one embodiment of a linearity measuring apparatus in accordance with the present invention, showing a state before a wafer is mounted on a platform;

FIG. 2 is a plan view corresponding to FIG. 1, showing a state in which a wafer is mounted on a platform and a first Ori-Fla of the wafer is allowed to abut against a block;

FIG. 3 is a plan view corresponding to FIG. 1, showing a state in which a block is separated from [redacted] Ori-Fla of the wafer;

FIG. 4 is a plan view corresponding to FIG. 1, showing a state in which a platform is moved together with a wafer [redacted] to bring the Ori-Fla into [redacted];

FIG. 5 is a sectional view taken along the line A-A of FIG. 2;

FIG. 6 is a sectional view taken along the line B-B of FIG. 3;

FIG. 7 is a sectional view taken along the line C-C of FIG. 4; and

FIG. 8 is a plan view of a wafer in which the fabrication accuracy of the Ori-Fla is poor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be described with reference to the accompanying drawings.

As shown in FIGS. 1 and 5, three straight tracks 11a such as linear motion guides (LM guides) are formed in a base 11 of a linearity measuring apparatus 10 so as to extend in a first direction, and a platform 13 engages with these straight tracks 11a via engagement means 12. This engagement means 12 has a fixed rail 14 and a movable rail 16 as shown in detail in FIG. 5. The fixed rail 14 is fixed by being inserted in the straight track 11a, and the movable rail 16 is fixed by being inserted in a groove 13a formed in the bottom surface of the platform 13 and is fitted on the fixed rail 14 via needle-shaped rollers 17. The fixed rail 14 is formed with a convex portion 14a that projects upward and extends in the [redacted] direction of the rail 14. The movable rail 16 is formed with a concave portion 16a that has a cross-sectional shape

corresponding to the convex portion 14a and a size larger than the convex portion 14a and extends in the [redacted] direction of the rail 16. The needle-shaped roller 17 is configured so as to rotatively slide on the movable rail 16 and rolls on the fixed rail 14. Thereby, the movable rail 16 is configured so as to move in the first direction along the fixed rail 14 or the straight track 11a together with the platform 13. The top surface of the platform 13 is formed so as to be flat so that a wafer 18 is mounted. The wafer 18, having a diameter [redacted] of 50 to 300 mm, has a first Ori-Fla 18a and a second Ori-Fla 18b. The number of [redacted] tracks is not limited to three, and may be one, two, [redacted]. Also, the fixed rail may be formed with a concave portion, not the convex portion, and the movable rail may be formed with a convex portion, not the concave portion. Further, between the fixed rail and the movable rail, steel balls or sliding bearings may be interposed instead of the needle-shaped rollers.

On the other hand, a block 19 is provided on the base 11 with a predetermined first clearance L (FIG. 1) being provided with the straight track 11a in a second direction perpendicular to the first direction (FIGS. 1 and 5). This block 19 is installed to the base 11 via release means 21. The block 19 is formed with a flat face 19a that is parallel with the first direction and perpendicular to the top surface of the base 11 so that the first Ori-Fla 18a or the second Ori-Fla 18b of the wafer 18 [redacted]

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[redacted] can abut against the flat face 19a. The first clearance L is a clearance between the block 19 and the straight track 11a of the three straight tracks 11a which is closest to the block 19. This first clearance L is formed so as to be greater than the distance from the straight track 11a closest to the block 19 to the face of the platform 13 opposed to the block 19. As shown in detail in FIGS. 5 and 6, the release means 21 has a release body 22 installed on the base 11 behind the block 19, a rod 23 one end of which is inserted and fixed in the block 19 and the other end of which is slidably inserted in the release body 22, and an operating lever 24 the substantially central portion of which is [redacted] provided on the release body 22 via a first pin 31 and the lower end of which is connected to the other end of the rod 23 via a second pin 32.

A helical compression spring 26 is provided around the rod 23. One end of this spring 26 is pressed on the block 19, and the other end thereof is pressed on the release body 22. Further, a helical tension spring 27 is provided between the release body 22 and the operating lever 24. The lower end of this spring 27 is fixed to a lower pin 28 fixed to the release body 22, and the upper end thereof is fixed to an upper pin 29 fixed to the operating lever 24. The lower pin 28 is located on the vertical line passing through the first pin 31, and the upper pin 29 is located at an upper position separated a predetermined distance

from the first pin 31 in the [redacted] direction of the operating lever 24. The operating lever 24 is configured so as to be [redacted] between a first position (FIG. 5) at which the first Ori-Fla 18a or the second Ori-Fla 18b is allowed to abut against the flat face 19a of the block 19 and thereby the wafer 18 can be positioned and a second position (FIG. 6) at which the block 19 is separated from the first Ori-Fla 18a or the second Ori-Fla 18b, that is, the block 19 goes apart from the straight track 11a [redacted].

The spring constant of the helical tension spring 27 is set so as to be larger than that of the helical compression spring 26. Therefore, when the operating lever 24 is operated to the second position, the elastic force of the helical tension spring 27 overcomes that of the helical compression spring 26, so that the helical tension spring 27 can temporarily [redacted] at the second position. Reference numeral 33 in FIGS. 5 and 6 denotes a flat bar fixed to the base 11 in parallel with the straight track 11a. This flat bar 33 has a function such that when the operating lever 24 is operated to the first position (FIG. 5), the flat face 19a of the block 19 abuts against the flat bar 33, by which the flat face 19a of the block 19 is corrected so as to become parallel with the straight track 11a. Also, reference numeral 24a denotes an elongated hole formed in a lower end portion of the operating lever 24 so that the second pin 32 is

inserted in this elongated hole 24a.

On the other hand, the platform 13 is provided with wafer fixing means 34 for fixing the wafer 18 in a state in which the wafer 18 is mounted on the platform 13 (FIGS. 1 and 5). This wafer fixing means 34 includes a suction port 36 for attracting and fixing the wafer 18, which is formed in the top surface of the platform 13, a suction hole 37a one end of which communicates with the suction port 36, which is formed in the platform 13, a suction pipe 37b one end of which is connected to the other end of the suction hole 37a and the other end of which is connected to a vacuum supply (not shown), a switching valve (not shown) for switching the suction port 36 to a negative pressure or the atmospheric pressure, which is provided in the suction pipe 37b, and a selector switch 38 for turning on/off the switching valve. The suction hole 37a and the suction pipe 37b constitute a suction passage 37. The switching valve, which is an electromagnetic valve for 3-port 2-position switching, is configured so that when the selector switch 38 is turned on, the suction port 36 communicates with the vacuum [redacted] to provide a negative pressure, and when the selector switch 38 is turned off, the suction port 36 communicates with the atmosphere to provide the atmospheric pressure. Also, a [redacted] having a probe 39a at the tip end of a spindle 39d is installed on the base 11 (FIGS. 1 to 4 and 7). This [redacted] 39 is located on the base 11 with a

predetermined second clearance M (FIG. 1) being provided with the block 19 in the first direction, and is configured so that the probe 39a can be displaced in the second direction in such a manner as to be opposed to the straight track 11a. At the tip end of the probe 39a, there is provided a steel ball 39b capable of rolling on the first Ori-Fla 18a or the second Ori-Fla 18b. Taking a clearance between the tip end of the probe 39a and the straight track 11a as N, the [redacted] 39 is fixed on the base 11 so that the following equation (1) is satisfied.

[redacted]

A method for using an apparatus 10 for measuring the linearity of the first Ori-Fla 18a of the wafer 18, which is constructed as described above, will be described with reference to FIGS. 1 to 7.

First, the selector switch 38 is turned off, and the platform 13 on which the wafer is not mounted is moved in the first direction so that the platform 13 is opposed to the block 19. Then, the operating lever 14 is operated to the first position (FIG. 5) to cause the flat face 19a of the block 19 to abut against the flat bar 33 (FIG. 1). Next, a wafer 18 is mounted on the top surface of the platform 13, and the first Ori-Fla 18a of the wafer 18 is caused to abut against the flat face 19a of the block 19 in such a manner as to be parallel with the flat face 19a (FIGS. 2 and 5). In this state, the selector switch 38 is

turned on to cause the suction port 36 to communicate with the vacuum [redacted], by which the wafer 18 is attracted and fixed onto the platform 13. Next, the operating lever 24 is turned from the first position (FIG. 5) to the second position (FIG. 6) to move the block 19 in the second direction so as to be separated from the wafer 18 (FIGS. 3 and 6). In this state, the platform 13 on which the wafer 18 is mounted and fixed is moved in the first direction, by which the first Ori-Fla 18a is brought into [redacted] with the tip end of the probe 39a of the [redacted] 39 (FIGS. 4 and 7). When the platform 13 is further moved in the first direction, the steel ball 39b at the tip end of the probe 39a of the [redacted] 39 rolls on the first Ori-Fla 18a, and [redacted] deflects. The deflection of the [redacted] 39c of the [redacted] 39 [redacted] the steel ball 39b at the tip end of the probe 39a of the [redacted] one end of the first Ori-Fla 18a to the other end thereof. The acceptability or non-acceptability of linearity of the first Ori-Fla 18a of the wafer 18 can be judged according to whether or not the deflection is within [redacted], for example, 25 μm. When the linearity of the first Ori-Fla 18a of another wafer 18 is measured succeedingly, the selector switch 38 is turned off, and the wafer 18 having been subjected to measurement is removed from the platform 13. Thereafter, the above-described

procedure is repeated. In this manner, the linearity of the first Ori-Fla 18a of the wafer 18 can be measured accurately in a short period of time.

Although the linearity of the first Ori-Fla is measured by using the linearity measuring apparatus in the above-described embodiment, the linearity of the second Ori-Fla may [redacted] be measured [redacted]. [redacted] in the above-described embodiment, the deflection [redacted] is read visually. However, if the linearity measuring apparatus is configured so that the deflection data of [redacted] can be outputted as an electronic signal, the Ori-Fla linearity data for each wafer can be stored by connecting the [redacted] signal to the input of a computer, and also the acceptability or non-acceptability of [redacted] linearity of [redacted] Ori-Fla can be [redacted] by means of the computer when the apparatus of the present invention is automated.

The present invention achieves the following effects: as described above, according to the present invention, the platform is moved in the first direction so as to be opposed to the block, a wafer is fixed on the platform so that the Ori-Fla abuts against the block, [redacted] and the platform is moved in the first direction so that the Ori-Fla is brought into [redacted] with the probe of the [redacted] device, [redacted]. Therefore,

by reading the deflection of the [redacted] of the [redacted] the other end thereof, the linearity of the Ori-Fla can be displayed quantitatively as numerical [redacted] that the acceptability or non-acceptability of linearity of the Ori-Fla of the wafer can be [redacted]. As a result, the linearity of the Ori-Fla of the wafer can be measured accurately in a short period of time.

Also, if the wafer fixing means has the suction port for attracting and fixing the wafer, the suction passage communicating with the suction port, and the switching valve for switching the suction port to a negative pressure or the atmospheric pressure, the wafer can be fixed on the platform by a very simple operation without damage to the wafer.

Also, if the release means for moving the block in the second direction in which the block [redacted] from the straight track is provided, the Ori-Fla moves in a state of being separated from the block when the platform with the wafer being mounted thereon is moved in the first direction. As a result, the wafer is not damaged.

Further, if the linearity measuring apparatus is configured so that the deflection data of [redacted] can be outputted as an [redacted] signal, the Ori-Fla linearity data for each wafer can be stored by connecting the [redacted] signal to the input of a computer, and also the acceptability or non-acceptability of

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linearity of [redacted]Dri-Fla can be [redacted] by means of the computer when the apparatus of the present invention is automated.

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WHAT IS CLAIMED IS:

1. A linearity measuring apparatus for a wafer orientation flat, comprising:

a base in which [redacted] straight tracks are formed in a first direction;

a platform which is configured so as to be movable in said first direction by being engaged with said straight track via engagement means, and is further provided with a top surface formed so as to be flat to mount a wafer having an orientation flat;

a block which is installed on said base with a predetermined first clearance L being provided with the straight track in a second direction perpendicular to said first direction, and has a flat face against which the orientation flat of said wafer mounted on said platform abuts and which is parallel with said first direction;

wafer fixing means provided in said platform to fix said wafer in a state in which said wafer is mounted on said platform; and

a [redacted] which is installed on said base with a predetermined [redacted] clearance M being provided with said block in said first direction, and has a probe opposed to said straight track and capable of being displaced in said second direction, wherein

when a clearance between the tip end of said probe and said straight track is taken as N, the following equation [redacted] is satisfied

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[redacted] .....

2. The linearity measuring apparatus according to claim 1, wherein said wafer fixing means has a suction port formed in said platform to attract and fix said wafer, a suction passage communicating with said suction port, and a switching valve provided in said suction passage to switch said suction port to a negative pressure or the atmospheric pressure.

3. The linearity measuring apparatus according to claim 1, wherein release means for moving said block in said second direction in which said block goes apart from said straight track is [redacted].

4. The linearity measuring apparatus according to claim 1, wherein deflection data [redacted] can be outputted as an [redacted] signal.

5. The linearity measuring apparatus according to claim 1, wherein said apparatus can be applied to a wafer having a diameter in the range of 50 to 300 mm.

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ABSTRACT OF THE DISCLOSURE

Straight tracks are formed in a first direction on a base. The top surface of a platform is formed so as to be flat to mount a wafer having an Ori-Fla, and the platform is moved in the first direction by being engaged with the straight tracks via engagement means. A block having a flat face against which the Ori-Fla of the wafer abuts and which is parallel with the first direction is installed with a first clearance L being provided with the straight track in a second direction perpendicular to the first direction. Wafer fixing means for fixing the wafer in a state in which the wafer is mounted on the platform is provided in the platform, and a [redacted] having a probe opposed to the straight track and capable of being displaced in the second direction is installed [redacted] with a second clearance M being provided with the block in the first direction. When a clearance between the tip end of the probe and the straight track is taken as N, the relationship of [redacted] exists. By this configuration, the linearity of the Ori-Fla can be measured accurately in a short period of time.

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FIG. 1

FIG. 2

FIG. 3

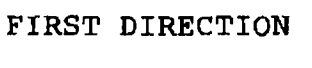
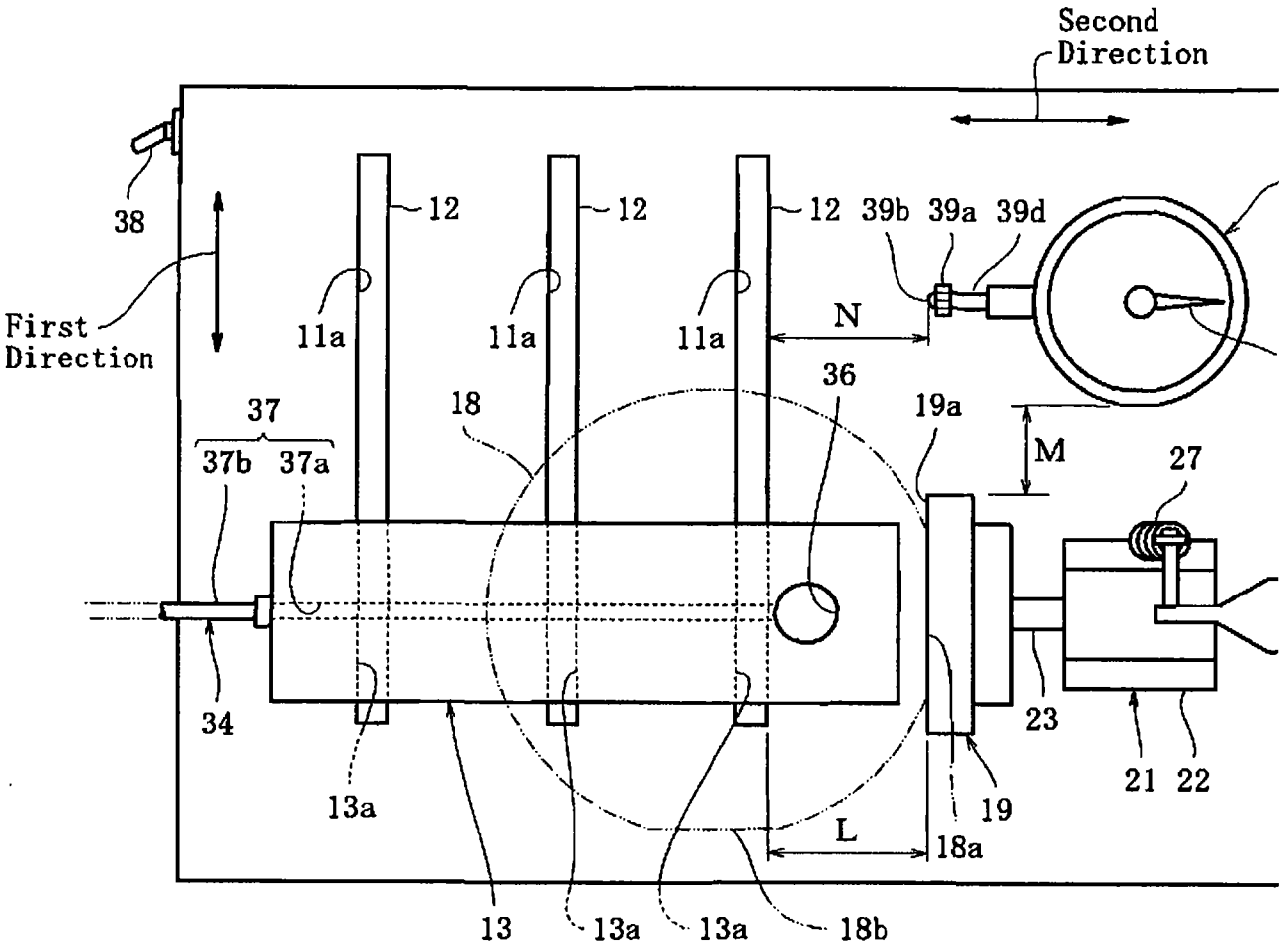


FIG. 4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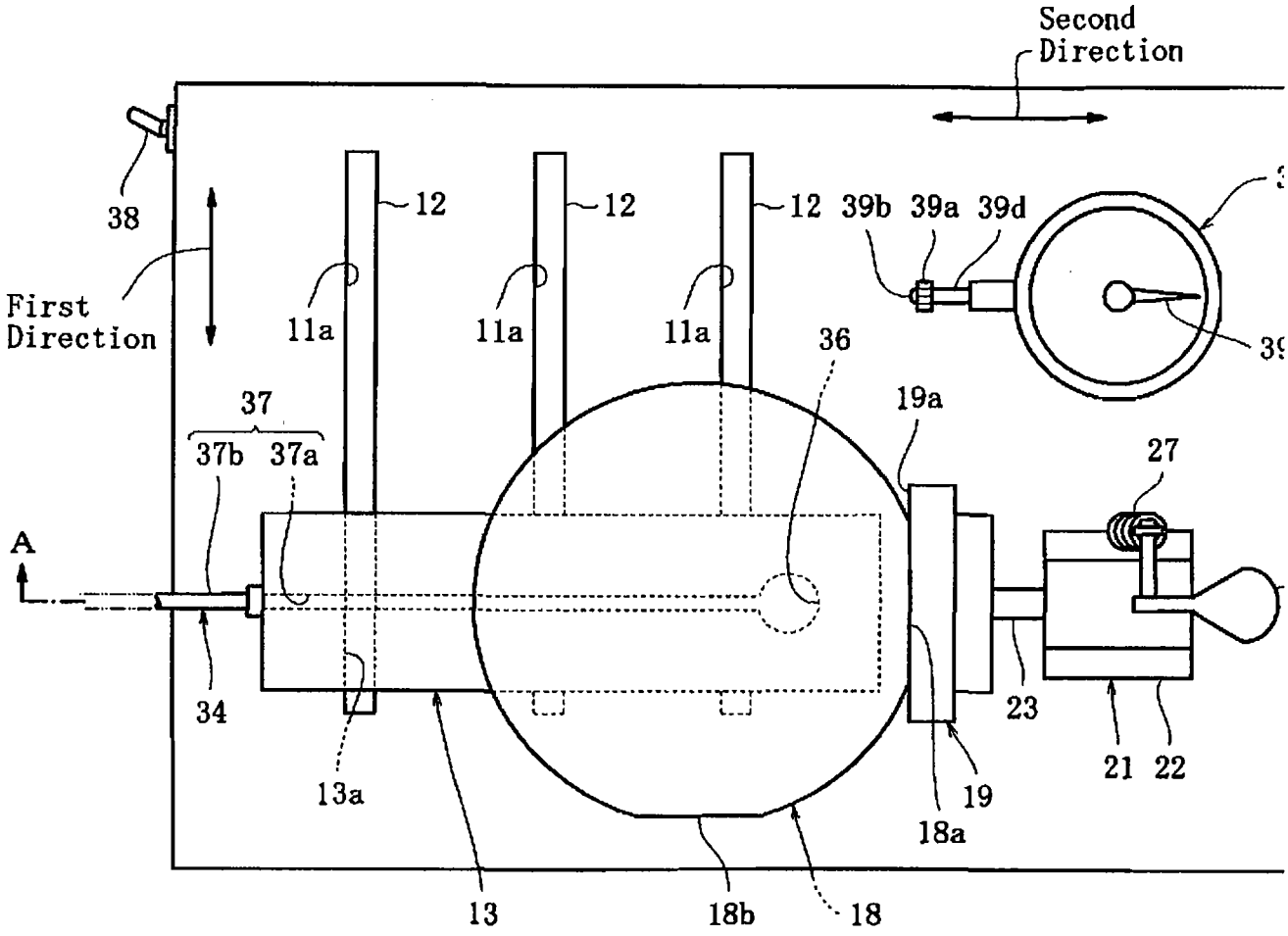
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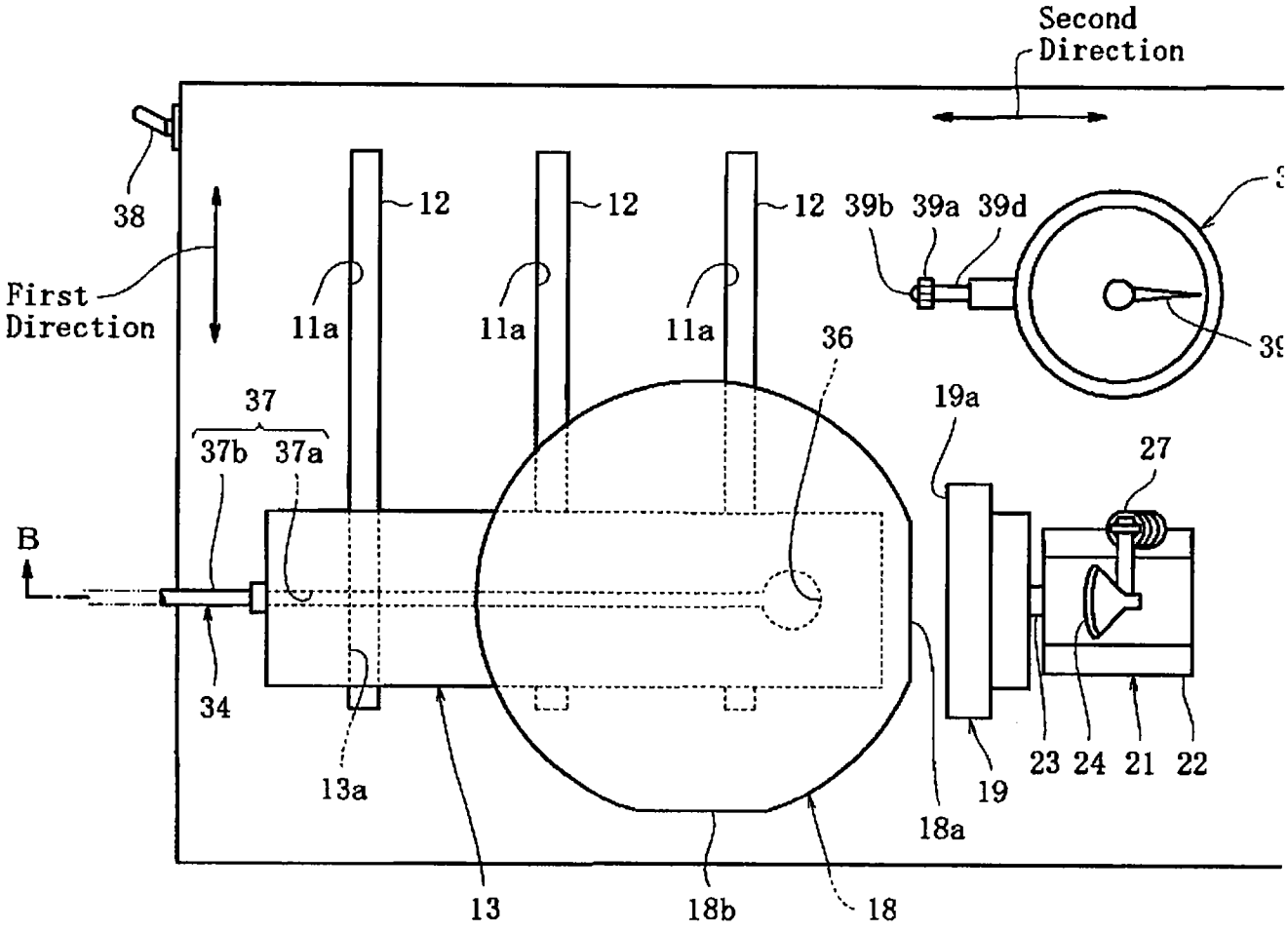
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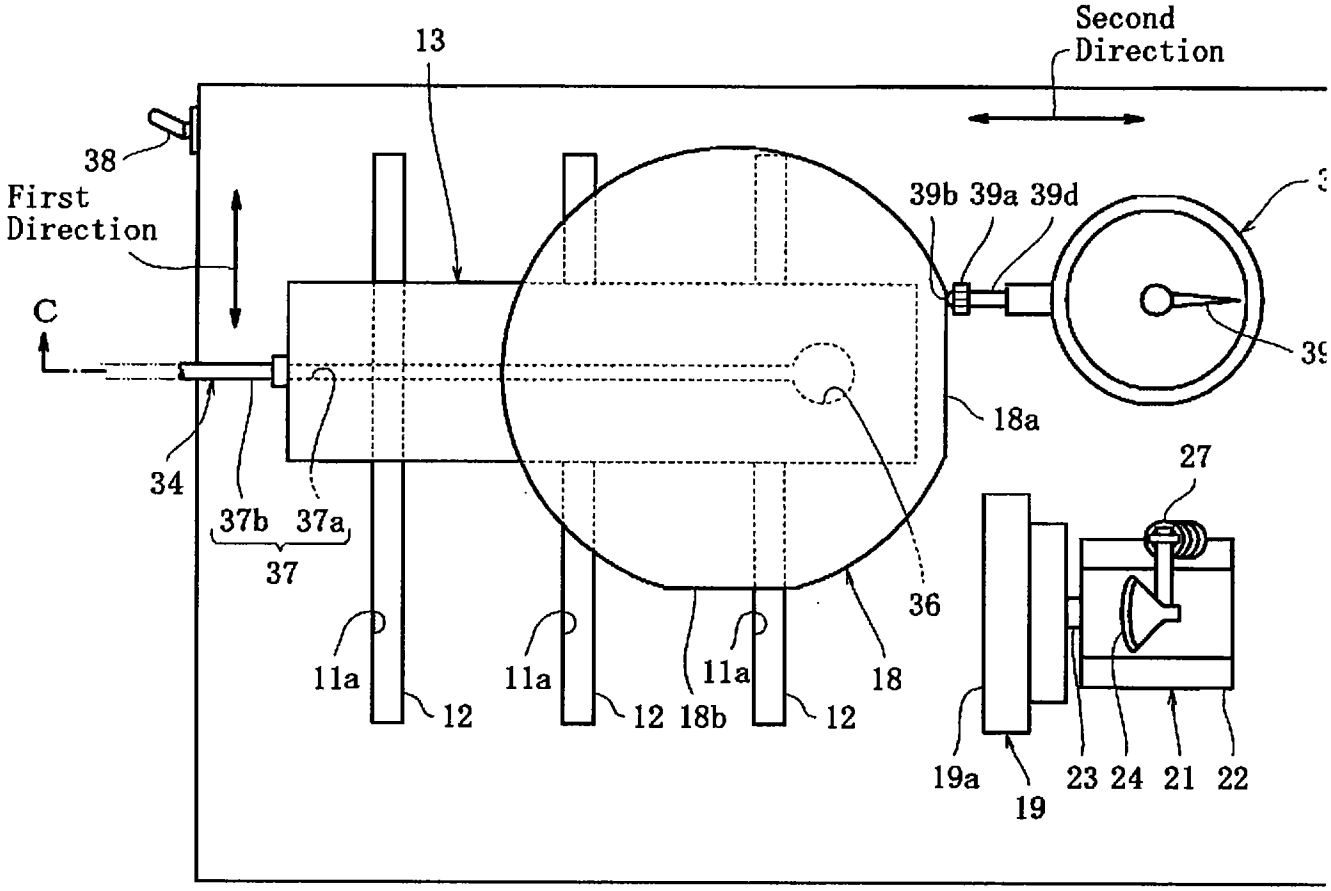
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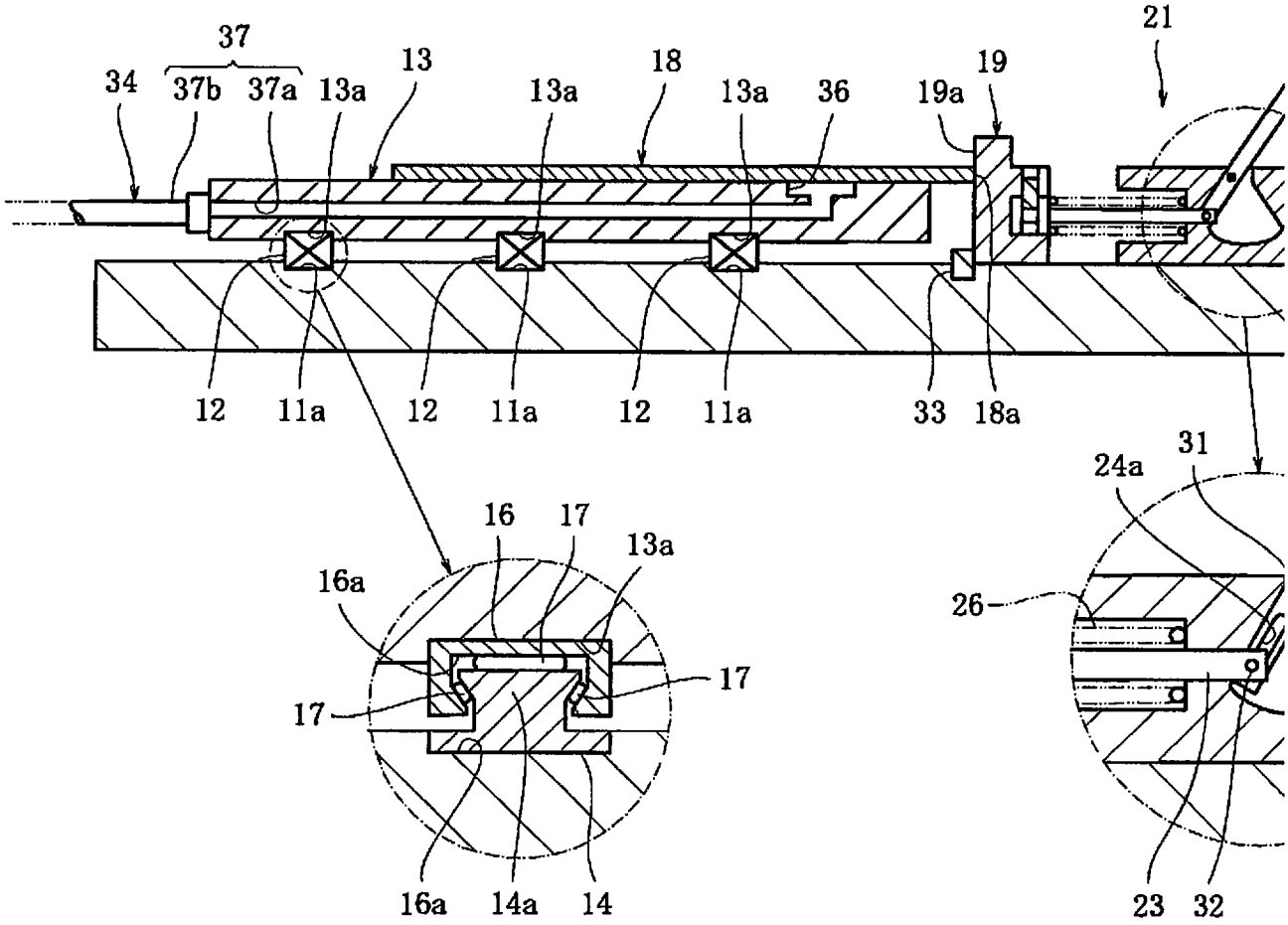
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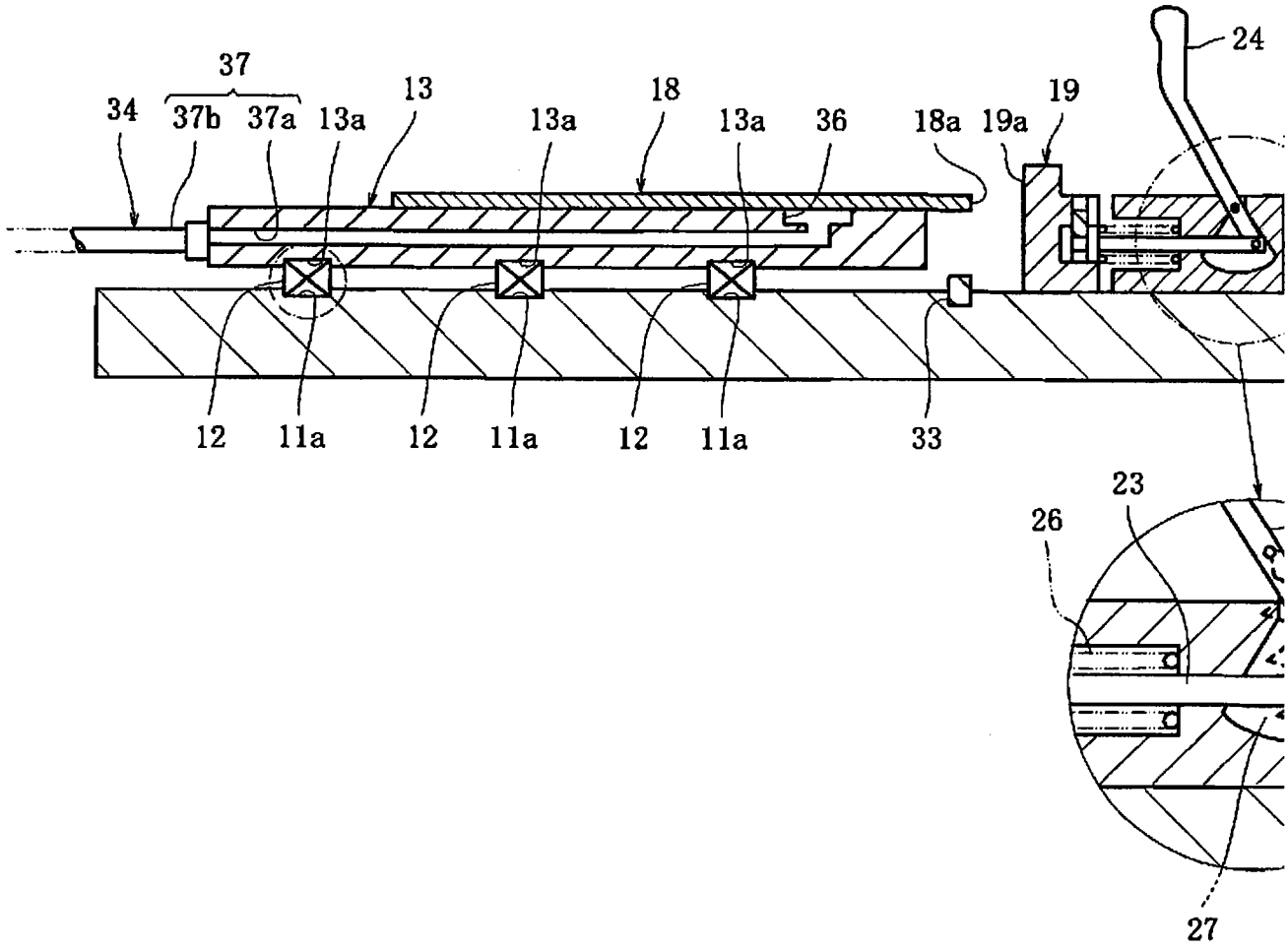
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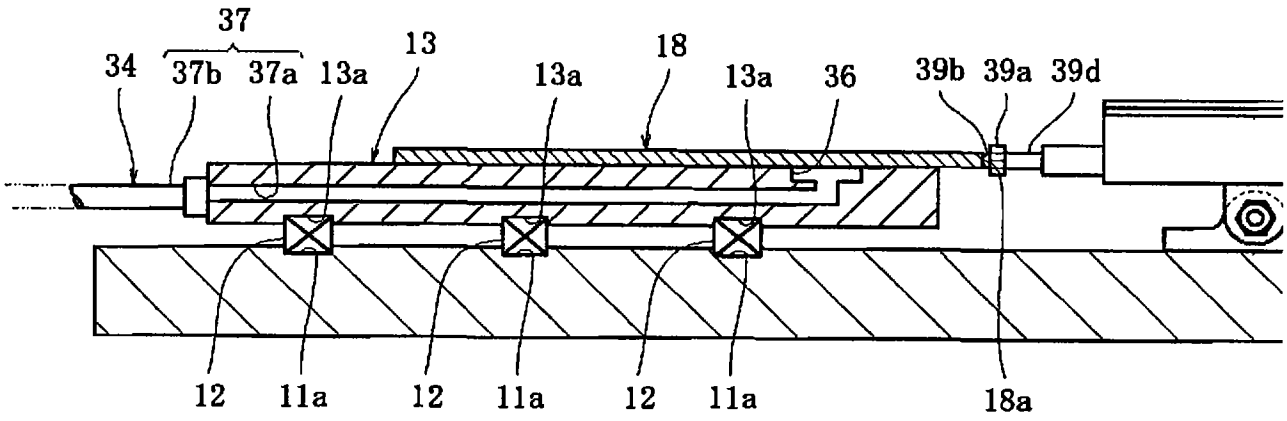
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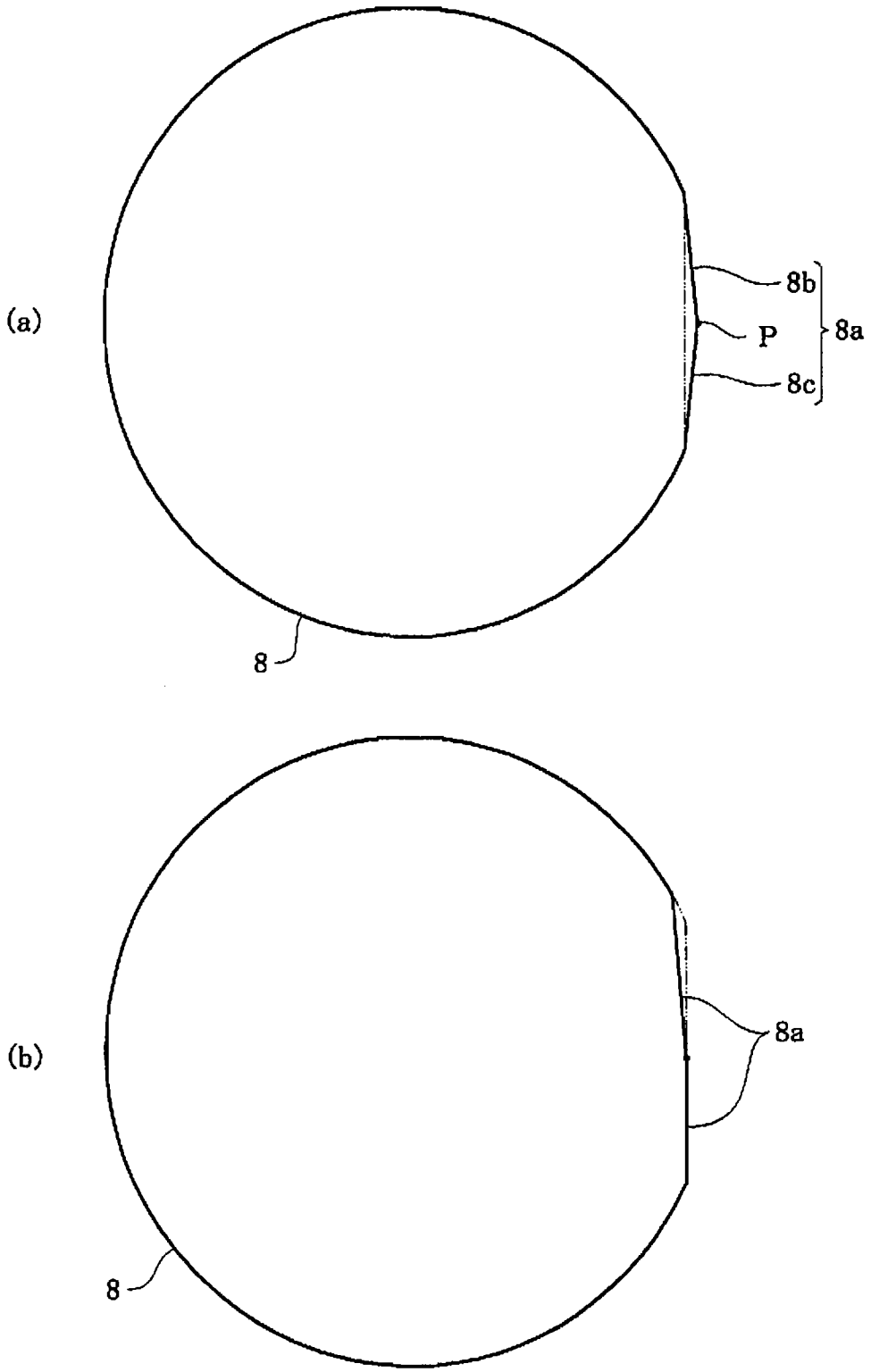
EXHIBIT 7

Fig. 8



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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
09/904,425	07/12/2001	Cindy Kohanek	JG-SU-5072

CONFIRMATION NO. 1776


OC000000009284155

REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
New York, NY 10152

Title: Linearity measuring apparatus for wafer orientation flat

Publication No. US-2002-0189118-A1
Publication Date: 12/19/2002

Date Mailed: 12/19/2002

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,425	07/12/2001	Cindy Kohanek	JG-SU-5072	1776

7590 07/03/2002

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EXAMINER
BENNETT, GEORGE B

ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 07/03/2002

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DOCKET
DUE Oct. 3 2002 Reply Due
Jan. 3, 2003 Reply Deadline

PTO-90C (Rev. 07-01)

C002

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EXHIBIT X

Office Action Summary	Application No.	Applicant(s)	
	09/904,425	KOHANEK ET AL.	
	Examiner	Art Unit	
	G. Bradley Bennett	2859	

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- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2001* .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the electronic signaling device (claim 4) must be shown or the feature(s) canceled from the claim(s). Currently, only an analog dial gauge is shown. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

3. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 3: the term "one, two, or more" is indefinite. Furthermore, only an embodiment with three tracks is shown in the figures. Please clarify.

Claim 1, last line: The claim appears to end with an equation, however, there is no period at the end of the claim. Please clarify whether or not the equation is the end of the claim.

Conclusion

4. Claims 1-3 and 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Bradley Bennett whose telephone number is 703.308.1284. The examiner can normally be reached on M-TH 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F.F. Gutierrez can be reached on 703.308.3875. The fax phone numbers for the organization where this application or proceeding is assigned are 703.308.7722 for regular communications and 703.308.7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.308.0956.

G. Bradley Bennett
Primary Examiner
Art Unit 2859

gbb
June 30, 2002

EXHIBIT 7

Notice of References Cited	Application/Control No. 09/904,425	Applicant(s)/Patent Under Reexamination KOHANEK ET AL.	
	Examiner G. Bradley Bennett	Art Unit 2859	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A'	US-4,680,865	07-1987	Danielli et al.	33/549
	B	US-4,833,790	05-1989	Spencer et al.	33/549
	C	US-5,205,046	04-1993	Barnett et al.	33/533
	D	US-5,433,013	07-1995	Woodhouse, Glenn P.	33/533
	E	US-5,539,992	07-1996	Woodhouse, Glenn P.	33/533
	F	US-5,639,953	06-1997	Renslow, Bruce E.	33/533
	G	US-6,148,532	11-2000	Ellis, Robert W.	33/533
	H	US-6,185,830	02-2001	Walters, Frank Stephen	33/533
	I	US-6,195,905	03-2001	Cole, Jerry W.	33/533
	J	US-6,408,532	06-2002	Keys et al.	33/549
	K	US-			
	L	US-			
	M'	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U'	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Quality Assurance Specialists:
Don Hajec.....703-308-4075 **Paul Dzierzynski.....703-308-4822**

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Directors, Technology Center 2800
Semi-conductors, Electrical, Optical Systems & Components

Sharon Gibson	703/308-0658	2810
Rolf G. Hille	703/306-0658	2820
Richard Seidel	703/306-3431	2830/40
Howard N. Goldberg	703/306-3431	2850/60
Janice A. Falcone	709/308-0530	2870/80

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MAY 24, 2002

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JULES E. GOLDBERG, ESQ.
375 PARK AVENUE
NEW YORK, NEW YORK 10152

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RECORDATION DATE: 03/11/2002

REEL/FRAME: 012730/0063
NUMBER OF PAGES: 2

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
KOHANEK, CINDY

DOC DATE: 12/03/2001

ASSIGNOR:
BABB, GARY

DOC DATE: 12/03/2001

ASSIGNEE:
MITSUBISHI MATERIALS SILICON
CORPORATION
5-1, OHTEMACHI 1-CHOME, CHIYODA-KU
TOKYO 100-0004, JAPAN

ASSIGNEE:
MITSUBISHI SILICON AMERICA
CORPORATION
2445 FABER PLACE
SUITE 100
PALO ALTO, CALIFORNIA 94303-0912

SERIAL NUMBER: 09904425
PATENT NUMBER:

FILING DATE: 07/12/2001
ISSUE DATE:

C009

MARCUS KIRK, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

ASSIGNMENT OF PATENT APPLICATION

EXHIBIT

UNITED STATES OF AMERICA

Whereas, I/We, Cindy Kohanek and Gary Babb

of c/o Mitsubishi Silicon America Corporation, 1351 Tandem Avenue N.E., Salem, Oregon 97303 U.S.A.

(hereafter "Assignor") have new and useful improvements in LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

which application for Letters Patent in the United States of America | | is about to be filed. |X| has been filed.

And Whereas, MITSUBISHI MATERIALS SILICON CORPORATIION and MITSUBISHI SILICON AMERICA CORPORATION

of 5-1, Ohtemachi 1-chome, Chiyoda-ku, Tokyo 100-0004 Japan
2445 Faber Place, Suite 100, Palo Alto, California 94303-0912, U.S.A.

(hereinafter "Assignee") is/are desirous of acquiring an interest therein and in the Letters Patent to be obtained therefor:

Now, therefore, be it known by all whom it may concern, that for good and valuable consideration (the sufficiency of which is hereby acknowledged) the Assignor has assigned, transferred and set over, and by these presents does assign, transfer and set over unto the said Assignee for the territory of the United States of America, the full and exclusive right, title, and interest in and to the said application and the invention embodied therein, as fully set forth and described in the specification.

A. prepared and executed on _____

B. filed in the U.S. Patent and Trademark Office under Serial No. 09/904,425 on July 12, 2001 including any division, continuation, substitute or renewal application thereof; said invention, application and Letters Patent to be held and enjoyed by the said Assignee to the full end of the term for which said Letters Patent is granted, as fully and entirely as the same would have been held by the Assignor had this assignment and transfer not been made.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue any and all such Letters Patent for said invention to said Assignee.

In testimony whereof, the Assignor has hereunto set his hand this 3rd day of December 2001.

WITNESS:	INVENTOR(S):	
	Cindy Kohanek	Cindy Kohanek
	(Name of Assignor)	(Signature of Assignor)
	Gary Babb	
	(Name of Assignor)	(Signature of Assignor)
		/
	(Name of Assignor)	(Signature of Assignor)
		/
	(Name of Assignor)	(Signature of Assignor)
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EXECUTION DATE: December 3, 2001

Name of conveying Party(ies):
Cindy KOHANEK
Gary BABB

Execution Date (M / D / Y):
December 3, 2001
December 3, 2001

Name of receiving Party(ies): **MITSUBISHI MATERIALS SILICON CORPORATION and MITSUBISHI SILICON AMERICA CORPORATION**

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Name of Person Signing

Signature

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[ ] Merger [ ] Security Agreement
[ ] Other:
EXECUTION DATE: December 3, 2001

Name of conveying Party(ies): Execution Date (M / D / Y):
Cindy KOHANEK **December 3, 2001**
Gary BABB **December 3, 2001**

Name of receiving Party(ies): **MITSUBISHI MATERIALS SILICON CORPORATION and MITSUBISHI SILICON AMERICA CORPORATION**

Address of receiving Party(ies): **5-1, Ohtemachi 1-chome, Chiyoda-ku, Tokyo 100-0004 Japan**
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Deposit Account Number: 50-1529
Authorization to charge additional fees [ ] Yes [ ] No

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,425	07/12/2001	Cindy Kohanek	JG-SU-5072	1776

7590 07/03/2002

REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
New York, NY 10152

EXAMINER	
BENNETT, GEORGE B	
ART UNIT	PAPER NUMBER
2859	

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DUE Oct. 3, 2002 Reply Due
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PTO-90C (Rev. 07-01)

C014

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Office Action Summary	Application No.	Applicant(s)	
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	Examiner	Art Unit	
	G. Bradley Bennett	2859	

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- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the electronic signaling device (claim 4) must be shown or the feature(s) canceled from the claim(s). Currently, only an analog dial gauge is shown. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

3. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 3: the term "one, two, or more" is indefinite. Furthermore, only an embodiment with three tracks is shown in the figures. Please clarify.

Claim 1, last line: The claim appears to end with an equation, however, there is no period at the end of the claim. Please clarify whether or not the equation is the end of the claim.

Conclusion

4. Claims 1-3 and 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Bradley Bennett whose telephone number is 703.308.1284. The examiner can normally be reached on M-TH 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F.F. Gutierrez can be reached on 703.308.3875. The fax phone numbers for the organization where this application or proceeding is assigned are 703.308.7722 for regular communications and 703.308.7722 for After Final communications.

Col7

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.308.0956.

G. Bradley Bennett
Primary Examiner
Art Unit 2859

gbb
June 30, 2002

EXHIBIT 7

Notice of References Cited	Application/Control No. 09/904,425	Applicant(s)/Patent Under Reexamination KOHANEK ET AL.	
	Examiner G. Bradley Bennett	Art Unit 2859	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A'	US-4,680,865	07-1987	Danielli et al.	33/549
	B	US-4,833,790	05-1989	Spencer et al.	33/549
	C	US-5,205,046	04-1993	Barnett et al.	33/533
	D	US-5,433,013	07-1995	Woodhouse, Glenn P.	33/533
	E	US-5,539,992	07-1996	Woodhouse, Glenn P.	33/533
	F	US-5,639,953	06-1997	Renslow, Bruce E.	33/533
	G	US-6,148,532	11-2000	Ellis, Robert W.	33/533
	H	US-6,185,830	02-2001	Walters, Frank Stephen	33/533
	I	US-6,195,905	03-2001	Cole, Jerry W.	33/533
	J	US-6,408,532	06-2002	Keys et al.	33/549
	K	US-			
	L	US-			
	M'	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U*	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Dear United States Patent and Trademark Office Customer:

Quality and customer satisfaction are important to Technology Center 2800.

Technology Center 2800 has taken continuous quality improvement efforts to ensure that the accompanying correspondence meets high quality standards, and focuses on good customer service. It is important to us that you are satisfied with the services we provide.

If the communication you have received has any issues that raise concerns as to the quality and/or clarity of the action taken by the examiner, we invite you to contact the appropriate Supervisory Primary Examiner. You may also contact one of our Quality Assurance Specialists.

Quality Assurance Specialists:
Don Hajec.....703-308-4075 **Paul Dzierzynski.....703-308-4822**

If the contents of the attached correspondence have any clerical omissions, e.g., missing references or pages, illegible text, or any other similar errors, please contact us at the number below. We will take appropriate action to expedite the necessary corrections. Also, if you have general questions concerning any application assigned to Technology Center 2800, please contact our Customer Service Center. Questions concerning the merits of the application must be directed to the Examiner in charge of the particular application, then to the supervisor if appropriate.

TC 2800Customer Service Center **Crystal Plaza 4-6th floor, D-corridor**

Customer Service Representatives:
Linda M. Hodge-Taylor **CP4-6-D32**
Wynette Stapor **CP4-6-D30**

The Customer Service Center is open to receive requests for service in person, by phone **703-306-3329**, or Fax **703-306-5515**, from 8:30 am- 5:00 p.m. each business day.

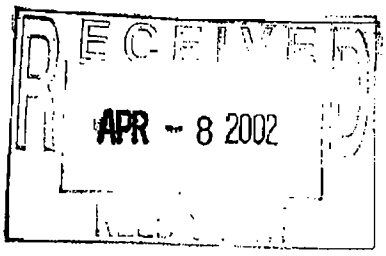
Attention: Policy on Returning Telephone Calls
USPTO-wide customer service standards state that if a USPTO employee being called is not available, they will return your call by the next business day, or, if you request, an alternate point of contact will be provided. Technology Center 2800 is committed to meeting this service standard. If you have called any employee in our Technology Center and have not received a return phone call within one (1) business day or have not been provided another point of contact, please contact our Customer Service Center at 703-306-3329. We ensure that you will receive a return phone call, from an employee with the ability to assist you, within four (4) business hours of this contact.

Any matter not satisfactorily resolved by the listed resources should be brought to the attention of the appropriate Director listed below. We appreciate your assistance in helping us help you.

Directors, Technology Center 2800
Semi-conductors, Electrical, Optical Systems & Components

Sharon Gibson	703/308-0658	2810
Rolf G. Hille	703/306-0658	2820
Richard Seidel	703/306-3431	2830/40
Howard N. Goldberg	703/306-3431	2850/60
Janice A. Falcone	709/308-0530	2870/80

EXHIBIT 7



Mailing Certificate / February 13, 2002 / BOX ASSIGNMENT

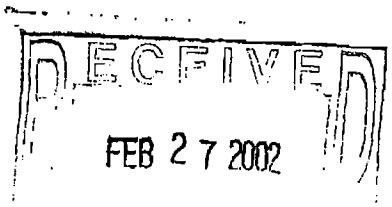
JG-SU-5072 / 500577 [illegible]0035
Cindy KOHANEK, ET AL.
09/904,425
Filing date July 12, 2001

OFFICE OF PUBLIC RECORDS
2002 MAR 11 PM 3:35
FINANCE SECTION

This to acknowledge receipt of the following:
Check for $ 40.00 #
PTO-1619A w/Assignment for Recordation.

c021

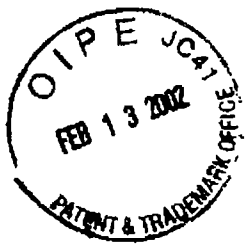
EXHIBIT 7



EXPRESS MAIL NO. EV 049 319 894 US / February 13, 2002
Box Missing Parts DUE DATE: FEBRUARY 28, 2002

JG-SU-5072 / 500577.20035
Cindy KOHANEK, et al.
09/904,425
Filing Date: July 12, 2001

This to acknowledge receipt of the following:
Check in the amount of $ 1440.00 # (4 month ext.)
Check in the amount of $ 130.00 # (Late Decl.)
Request for 4-month Extension
Completion of Application;
Executed Declaration;
Japanese Priority Document No: 2001-183702; and
Formalities Letter dated August 29, 2001



Status Request (to PTO)

12 April / July 2002

C022

EXPRESS MAIL No.: EV [redacted]319 894 US **EXHIBIT 7** Depos[redacted] **February 13, 2002**
hereby certify that this correspondence is being deposited with the United States Postal Service Express mail under 37 CFR 1.10 on the date indicated above and is addressed to: Box Missing, Commissioner for Patents, Washington, DC 20231

By: _____ / Ruth Montalvo Date: 02/13/02

In the event that this paper is late filed and a necessary Petition for an Extension of Time is not concurrently filed herewith, please consider this as a Petition for the requisite extension of time, and to the extent not tendered by check attached hereto, authorization to charge the extension fee, or any other fee required in connection with this paper, to Deposit Account No. 50-1529.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.	026418		
Docket No.	JG-SU-5072		
Applicant(s):	Cindy Kohanek, et. al.		
Application No.:	09/904,425	Group:	2856
Filed:	July 12, 2001	Examiner:	
For:	LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT		

BOX MISSING PARTS
Commissioner for Patents
Washington, D. C. 20231

RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Sir:

Applicants submit herewith the following in order to complete the above application:

(X) Executed Declaration and Power of Attorney.
( ) Verified English Translation.
( ) Applicant is entitled to claim Small Entity Status [See 37 CFR 1.27].
(X) Japanese Priority Document(s) No(s). 2001-183702 dated 18 JUNE 2001 the priority(ies) of which is(are) claimed under 35 USC 119.
(X) A copy of the Notice to File Missing Parts of Nonprovisional Application dated August 29, 2001.
(X) Check in the amount of $ 130.00.

With the filing of these documents, it is submitted that the application is now complete and in form for examination. Accordingly, such examination and favorable action are earnestly solicited.

Respectfully submitted,

February 13, 2002
Tel.No. (212) 521-5403

Jules E. Goldberg - Reg. No. 24,408
Reed Smith LLP
375 Park Avenue
New York, NY 10152

Enclosures:
as listed above

EXHIBIT 7

EXPRESS MAIL No.: **EV 049 319 894 US** Deposited: February 13, 2002
I hereby certify that this correspondence is being deposited with the United States Postal Service Express mail under 37 CFR 1.10 on the date indicated above and is addressed to: Box Missing Parts, Commissioner for Patents, Washington, DC 20231

/ **Ruth Montalvo** Date: February 13, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.	026418	
Docket No.:	JG-SU-5072 / 500577.20035	
Applicant(s):	Cindy KOHANEK and Gary BABB	
Serial No.:	09/904,425	Group: 2856
Filed:	July 12, 2001	Examiner:
For:	LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT	

Box MISSING PARTS
Assistant Commissioner for Patents
Washington, D. C. 20231

PETITION FOR A FOUR-MONTH EXTENSION

Sir:

Applicants hereby petition for a four-month extension of time to respond to the Missing Parts Office Action dated August 29, 2001.

A Completion of Application is filed concurrently herewith.

Enclosed is a check in the amount of $ 1440.00 is enclosed. The Commissioner is hereby authorized to charge any other fees required with this submission or to credit any over-payment to Deposit Account No. 50-1529.

Respectfully submitted,

JEG:dej
February 13, 2002
Tel.No. (212) 521-5403

Jules E. Goldberg - Reg. No. 24,408
Reed Smith LLP
375 Park Avenue
New York, NY 10152

EXHIBIT 7

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/904,425	07/12/2001	Cindy Kohanek	JG-SU-5072/500577.20035

CONFIRMATION NO. 1776

FORMALITIES LETTER

OC000000006489266

REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
New York, NY 10152

Date Mailed: 08/29/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

A copy of this notice MUST be returned with the reply.

H.T

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Docket No.:

EXHIBIT 7

DECLARATION FOR PATENT APPLICATION

As a below named inventor(s), I (we) hereby declare that:

My (our) residence(s), post office address(es) and citizenship(s) is (are) the same as stated below next to my (our) name(s).

I (we) believe I am (we are) an original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

the specification of which is attached hereto unless the following box is checked:

[X] was filed on July 12, 2001 as United States Application Number 09/904,425 or
PCT International Application Number _____
and was amended on _____ (If applicable).

I (we) hereby state that I (we) have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I (we) acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I (we) hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed:	
(Number)	(Country)	(Day/Month/Year)	YES	NO
2001-183702	Japan	18/6/2001	X	

I (we) hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

(Application Number) (Filing Date)

I (we) hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I (we) acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulation, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.)	(Filing date)	(STATUS-patented, pending, abandoned)

EXHIBIT 7

DECLARATION FOR PATENT APPLICATION

I (we) hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and to act in accordance with the instructions from Suda Patent Office:

Lloyd McAulay,	Reg. No. 20,423;	J. Harold Nissen,	Reg. No. 17,283;
Jules E. Goldberg,	Reg. No. 24,408;	Gerald H. Kiel,	Reg. No. 25,116;
Eugene LeDonne,	Reg. No. 35,930;	Stephen M. Chin,	Reg. No. 39,938;
Arthur Dresner,	Reg. No. 36,612;	Samir R. Patel,	Reg. No. 44,998

all of Reed Smith LLP, 375 Park Avenue, New York, New York 10152-1799

Address all telephone calls to: Jules E. Goldberg, Esq. at Telephone No. (212) 521-5400

Address all correspondence to: Jules E. Goldberg, Esq.
Reed Smith LLP
375 Park Avenue, New York, NY 10152-1799 U.S.A.

I (we) hereby declare that all statements made herein of my (our) own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or 1st inventor (given name, family name):	Cindy Kohanek		
Residence:	Oregon, U.S.A.	Citizenship:	U.S.A.
Post Office Address:	c/o Mitsubishi Silicon America Corporation, 1351 Tandem Avenue N.E., Salem, Oregon 97303 U.S.A.		

Inventor's signature: Cindy Kohanek Date: 01/29/02

Full name of 2nd inventor (given name, family name):	Gary Babb		
Residence:	Oregon, U.S.A.	Citizenship:	U.S.A.
Post Office Address:	c/o Mitsubishi Silicon America Corporation, 1351 Tandem Avenue N.E., Salem, Oregon 97303 U.S.A.		

Inventor's signature: [signature] Date: 12/3/01

Full name of 3rd inventor (given name, family name):			
Residence:		Citizenship:	
Post Office Address:			

Inventor's signature: _____ Date: _____

日　本　国　特　許　庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出願年月日
Date of Application: ２００１年　６月１８日

出願番号
Application Number: 特願２００１－１８３７０２

出願人
Applicant(s): 三菱マテリアルシリコン株式会社
ミツビシシリコンアメリカ　コーポレーション

２００１年　７月　５日

特許庁長官
Commissioner,
Japan Patent Office

及川耕造

C028

EXPRESS MAIL NO. EV 049 319 894 US / February 13, 2002
Bo[redacted]ssing Parts EXHIBIT DATE: FEBRUA[redacted]28, 2002

JG-SU-5072 / 500577.20035
Cindy KOHANEK, et al.
09/904,425
Filing Date: July 12, 2001

This to acknowledge receipt of the following:
Check in the amount of $ 1440.00 # (4 month ext.)
Check in the amount of $ 130.00 # (Late Decl.)
Request for 4-month Extension
Completion of Application;
Executed Declaration;
Japanese Priority Document No: 2001-183702; and
Formalities Letter dated August 29, 2001

FOR SECURITY PURPOSES, THE BORDER OF THIS DOCUMENT CONTAINS MICROPRINTING

09/904,425

REED SMITH LLP
ATTORNEYS AT LAW
375 Park Ave.
New York, NY 10152

1-8/210

1374

DATE 2-13-02

PAY TO THE ORDER OF Commissioner for Patents $ 130.00

One hundred thirty dollars — 00/100 DOLLARS

CITIBANK, N.A.

FOR 500577.20035

AUTHORIZED SIGNATURE

⑈001374⑈ ⑆021000089⑆ 587 03507026⑈

THIS DOCUMENT INCLUDES A SECURITY SCREEN ON BACK OF THE CHECK

FS

FOR SECURITY PURPOSES, THE BORDER OF THIS DOCUMENT CONTAINS MICROPRINTING

09/904,425

REED SMITH LLP
ATTORNEYS AT LAW
375 Park Ave.
New York, NY 10152

1-8/210

1373

DATE 2-12-02

PAY TO THE ORDER OF Commissioner for Patents $ 1,440.00

One Thousand four hundred fourty dollars — 00/100 DOLLARS

CITIBANK, N.A.

FOR 500577.20035

AUTHORIZED SIGNATURE

⑈001373⑈ ⑆021000089⑆ 587 03507026⑈

THIS DOCUMENT INCLUDES A SECURITY SCREEN ON BACK OF THE CHECK

FS

C629

equivalent to Form PTO-1619A

EXHIBIT 7

To the Hon. Commissioner of Patents and Trademarks Please record the attached original or copy thereof Docket No. **JG-SU-5072 / 500577.20035**	Affix bar code label here:

SUBMISSION TYPE: [X] New [ ] Resubmission (Non-Recordation) Document ID #____ [ ] Correction of PTO Error / Reel #____ /Frame #____ [ ] Corrective Document / Reel #____ / Frame #____	Nature of Conveyance: [X] Assignment [ ] Change of Name [ ] Merger [ ] Security Agreement [ ] Other: EXECUTION DATE: December 3, 2001

Name of conveying Party(ies): **Cindy KOHANEK** **Gary BABB**	Execution Date (M / D / Y): **December 3, 2001** **December 3, 2001**

Name of receiving Party(ies): **MITSUBISHI MATERIALS SILICON CORPORATION and MITSUBISHI SILICON AMERICA CORPORATION**

Address of receiving Party(ies): **5-1, Ohtemachi 1-chome, Chiyoda-ku, Tokyo 100-0004 Japan**
2445 Faber Place, Suite 100, Palo Alto, CA 94303-0912, USA

If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative designation is attached: ____ YES ____ NO
(DESIGNATIONS MUST BE A SEPARATE DOCUMENT FROM ASSIGNMENT)

Correspondence and/or Domestic Representative Name, Address and Phone No.:
Jules E. Goldberg, Esq., Reed Smith LLP, 375 Park Avenue, New York, NY 10152 [Tel. No. (212)521-5400]

DO NOT USE THIS SPACE

Pages — Enter the total number of pages of the attached conveyance document including any attachments: **[3]**

Application number(s) or Patent number(s):
Enter either the patent Application Number or the Patent Number (DO NOT ENTER BOTH NUMBERS for the same property)
A) Application number(s): 09/904,425 B) Patent number(s):

If this document is being filed together with a New Application, enter the date the patent application was signed by the first named executing inventor: (M/D/Y)

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned

Number of Properties — Enter the total number of properties involved: **[1]**

Fee Amount Fee Amount for Properties Listed (37 CFR 3.41): **$ 40.00**

Method of payment: [X] Enclosed [ ] Deposit Account
(The Commissioner is hereby authorized to charge the deposit account any additional fees required or to credit any overpayment to Deposit Account No: 50-1529.)

Deposit Account
Enter for payment by deposit account or if additional fees can be charge to the account.
Deposit Account Number: 50-1529
Authorization to charge additional fees [ ] Yes [ ] No

Statement and Signature To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Jules E. Goldberg — Signature — Date: February 13, 2002
Reg. No.: 24,408
Name of Person Signing

MAILING CERTIFICATE I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box ASSIGNMENTS, Patent and Trademarks Office, Washington, DC 20231 on February 13, 2002

/ Ruth Montalvo

ASSIGNMENT - PATENT APPLICATION
UNITED STATES OF AMERICA

EXHIBIT 7

Whereas, I/We, Cindy Kohanek and Gary Babb

of c/o Mitsubishi Silicon America Corporation, 1351 Tandem Avenue N.E., Salem, Oregon 97303 U.S.A.

(hereafter "Assignor") have new and useful improvements in LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

which application for Letters Patent in the United States of America | | is about to be filed. |X| has been filed.

And Whereas, MITSUBISHI MATERIALS SILICON CORPORATIION and MITSUBISHI SILICON AMERICA CORPORATION

of 5-1, Ohtemachi 1-chome, Chiyoda-ku, Tokyo 100-0004 Japan
2445 Faber Place, Suite 100, Palo Alto, California 94303-0912, U.S.A.

(hereinafter "Assignee") is/are desirous of acquiring an interest therein and in the Letters Patent to be obtained therefor:

Now, therefore, be it known by all whom it may concern, that for good and valuable consideration (the sufficiency of which is hereby acknowledged) the Assignor has assigned, transferred and set over, and by these presents does assign, transfer and set over unto the said Assignee for the territory of the United States of America, the full and exclusive right, title, and interest in and to the said application and the invention embodied therein, as fully set forth and described in the specification.

A. prepared and executed on _____

B. filed in the U.S. Patent and Trademark Office under Serial No. 09/904,425 on July 12, 2001 including any division, continuation, substitute or renewal application thereof; said invention, application and Letters Patent to be held and enjoyed by the said Assignee to the full end of the term for which said Letters Patent is granted, as fully and entirely as the same would have been held by the Assignor had this assignment and transfer not been made.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue any and all such Letters Patent for said invention to said Assignee.

In testimony whereof, the Assignor has hereunto set his hand this 3rd day of December 2001.

WITNESS:	INVENTOR(S):	
	Cindy Kohanek	Cindy Kohanek
	(Name of Assignor)	(Signature of Assignor)
	Gary Babb	
	(Name of Assignor)	(Signature of Assignor)
	(Name of Assignor)	(Signature of Assignor)
	(Name of Assignor)	(Signature of Assignor)
	(Name of Assignor)	(Signature of Assignor)

UNITED STATES PATENT AND TRADEMARK OFFICE

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WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/904,425	07/12/2001	Cindy Kohanek	JG-SU-5072/500577.20035

CONFIRMATION NO. 1776

FORMALITIES LETTER

OC000000006489266

REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
New York, NY 10152

Date Mailed: 08/29/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

A copy of this notice MUST be returned with the reply.

H.T

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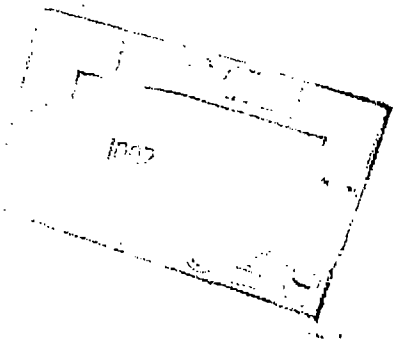
Initial Patent Examination Division (703) 308-1202
PART 1 - ATTORNEY/APPLICANT COPY

DUE Oct. 29, 2001 Executed Decl.
Feb. 28, 2002 Executed Decl. Deadline

C032



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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/904,425	07/12/2001	2856	710	JG-SU-5072/500577.20035	8	5	1

CONFIRMATION NO. 1776

FILING RECEIPT

OC000000006489265

REED SMITH LLP
Patent, Trademark and Copyright Matters
375 Park Avenue
New York, NY 10152

Date Mailed: 08/29/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Cindy Kohanek, Residence Not Provided;
Gary Babb, Residence Not Provided;

Assignment For Published Patent Application

Mitsubishi Materials Silicon Corporation;
Mitsubishi Silicon America Corporation;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2001-183702 06/18/2001

If Required, Foreign Filing License Granted 08/28/2001

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

C033

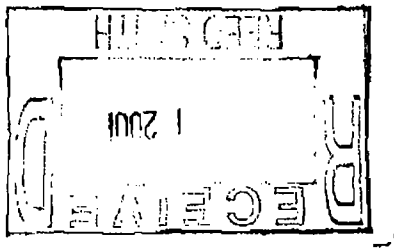

EXHIBIT 7

Linearity measuring apparatus for wafer orientation flat

Preliminary Class

073

Data entry by : TEGBARU, HAIMANOT **Team :** OIPE **Date:** 08/29/2001

C034

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Title 35, United States Code, Section 184
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- The title is recorded in sentence case.

Any corrections that may need to be done to your Filing Receipt should be directed to:

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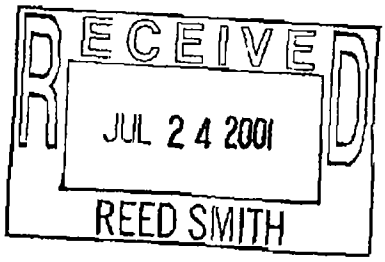
Washington, DC 20231

c035

EXHIBIT 7



09/904,425
JC

EXPRESS MAIL EL 915 669 445 US / July 12, 2001
JG-SU-5072 / 500577.20035 PATENT APPLICATION
PRIORITY: JUNE 18, 2001
Cindy KOHANEK and Gary BABB
LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

This is to acknowledge receipt of a New Patent Application as stated below:
Check in the amount of $ 710.00 # 0638
Transmittal;
LICENSE GRANTED: License Number: 527,026/Granted: June 1, 2001;
Preliminary Amendment Re: Pri); 15 pgs of Specification;
2 pgs of Claims (# 5/1); Abstract; and
Eight (8) sheets of Drawings (Fig. 1 - 8)

Executed Decl/POA - TO FOLLOW

DOCKET

DUE Nov. 12, 2001 mo. Def/on Rcvd?
Oct 12, 2001 Preliminary Amendment

C036

EXHIBIT 7

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Patent, Trademark and Copyright Matters

375 Park Avenue
New York, NY 10152
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EXPRESS MAIL No.: EL **915 669 445 US**
Deposited: **July 12, 2001**
I hereby certify that this correspondence is being deposited with the United States Postal Service Express mail under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, DC 20231

/ Ruth Montalvo

Commissioner for Patents
Washington, DC 20231

Date: **July 12, 2001**
Docket No: **JG-SU-5072 / 500577.20035**

Sir:

Transmitted herewith for filing is the Patent Application (37 CFR 1.53(b)) in the name(s) of:
Cindy KOHANEK and Gary BABB

FOR: **LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT**

ENCLOSED ARE:

(X) LICENSE GRANTED: **License Number: 527,026** **Granted: June 1, 2001**

(X) 15 pages of Specification, 2 page(s) of Claims (# of claims 5) & Abstract;

(X) Figs. 1 - 8 / Eight (8) sheet(s) of Drawings;

( ) Declaration and Power of Attorney; ***TO FOLLOW***

( ) PTO-1619A and an Assignment to: *Mitsubishi Materials Silicon Corporation and Mitsubishi Silicon America Corporation.*; ***TO FOLLOW***

( ) Certified copy(ies) of *Japanese Patent Appln No. 2001-183702 filed June 18, 2001*, the priority(ies) of which is(are) claimed under 35 USC 119; ***TO FOLLOW***

( ) Information Disclosure Statement, PTO-1449 and __ reference(s);

( ) Applicant is entitled to claim Small Entity Status [See 37 CFR 1.27];

(X) Preliminary Amendment.

THE FILING FEE HAS BEEN CALCULATED AS SHOWN BELOW:						
	Claims Filed		Extra	SMALL $ 355.00	LARGE $ 710.00	**AMOUNT $ 710.00**
Total Claims	**5**	Minus 20		x $ 9.00	x $ 18.00	
Independent	**1**	Minus 3		X $ 40.00	x $ 80.00	
[ ] Multiple dependent claim fee				+ $ 135.00	+ $ 270.00	
Assignment recordation fee ($ 40.00):						
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The Commissioner is hereby authorized to charge any additional fees associated with the filing of this application but not limited to: (X) Any patent application processing fees under 37 CFR 1.17
(X) Any filing fees under 37 CFR 1.16 for the presentation of extra claims
and any other fees required with this submission or to credit any overpayment to Deposit Account No. 50-1529.

Respectfully submitted

JEG:ram

Jules E. Goldberg - Reg. No. 24,408

C037

EXHIBIT 7

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SERIAL NUMBER	REQUEST DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
P-104,253	5/31/01	CINDY KOHANEK, ET AL	JG-SU-5072

Title: LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

Art Unit	Paper Number

Correspondence Address:
JULES E. GOLDBERG
REED SMITH LLP
375 PARK AVENUE, 17TH FL.
NEW YORK, NY 10152

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License Number: 527,026
Grant Date: 01-Jun-01

Approved:
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LICENSE FOR FOREIGN FILING

[Title 35, United States Code (1952) Sections 184, 185, 186]

EXHIBIT 7

EXPRESS MAIL No.: **EL 915 669 445 US** Deposited: **July 12, 2001**
I hereby certify that this correspondence is being deposited with the United States Postal Service Express mail under 37 CFR 1.10 on the date indicated above and is addressed to: Box Patent Application, Commissioner for Patents, Washington, DC 20231

By: _____ / Ruth Montalvo Date: 07/12/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.	026418
Docket No.	JG-SU-5072 / 500577.20035
Applicant(s):	Cindy KOHANEK and Gary BABB
Application No.:	
Filed:	Concurrently herewith - July 12, 2001
For:	LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

BOX Patent Application
Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

The above-identified application is filed concurrently herewith, please amend the specification as follows:

After the title and before BACKGROUND OF THE INVENTION insert the following:
--CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority of Japanese Application No. 2001-183702 filed June 18, 2001, the complete disclosure of which is hereby incorporated by reference. --

REMARKS

The above amendment is submitted to include the cross-referencing of the Japanese priority. No new matter is added. Entry into the application is earnestly solicited.

Respectfully submitted,

JEG:ram
July 12, 2001
Tel. (212) 521-5400

Jules E. Goldberg - Reg. No. 24,408
Reed Smith LLP
375 Park Avenue
New York, NY 10152

EXHIBIT 7

LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a measuring apparatus that provides numerical data relative to the linearity of an orientation flat (hereinafter referred to as an Ori-Fla).

Description of Related Art

Conventionally, examination of the linearity of an Ori-Fla portion has been by visual methodology, with no provision of quantitative data in which to make judgements. On the other hand, there has been disclosed a wafer Ori-Fla positioning method in which an Ori-Fla is positioned by pressing a wafer against a positioning mechanism provided on a wafer chuck mounting surface (Unexamined Japanese Patent Publication No. 10-22368). In this positioning method, the wafer chuck mounting surface is provided so as to be inclined, and a gas flow for floating a wafer with respect to a wafer chuck is generated by air blowing means.

In the positioning method configured as described above, when air is blown from the air blowing means in a state in which a wafer is mounted on the wafer chuck mounting surface, the wafer moves smoothly under gravity toward a positioning mechanism along the inclination of the wafer chuck mounting surface. As a result, the positioning of the Ori-Fla can be performed reliably.

Further, there has been disclosed an exposure device

that has a stage, a rough positioning mechanism, and number detecting means, and can perform exact rough positioning of a wafer without pattern at the time of first-level pattern exposure (Unexamined Japanese Patent Publication No. 8-78316). In this exposure device, at least three stopper members are provided to roughly position a wafer on the stage, and the stage moves in the longitudinal and transverse X & Y directions and in the rotation direction of θ. Also, the rough positioning mechanism performs rough positioning by causing the peripheral portions of wafer mounted on the stage to abut against the stopper members. Further, the number detecting means detects an identification number scribed on the wafer positioned roughly so that the wafer moves on the stage until the identification number arrives at a predetermined position.

In the conventional method in which the linearity of the Ori-Fla portion is examined visually, however, the acceptability or non-acceptability of linearity cannot be determined quantitatively. Also, in the conventional Ori-Fla positioning method disclosed in the aforementioned Unexamined Japanese Patent Publication No. 10-22368, or in the exposure device disclosed in Unexamined Japanese Patent Publication No. 8-78316, the fabrication accuracy of the Ori-Fla, especially the fabrication accuracy in chamfering the Ori-Fla is poor because the linearity of the Ori-Fla of wafer itself is not measured. For example, when as shown in FIG. 8(a), a vertex P is formed at the center of an Ori-

Fla 8a, and the Ori-Fla 8a is formed of a first side 8b and a second side 8c on opposite sides of the vertex P, there arises a problem in that the crystalline orientation of a wafer 8 deflects comparing the time when the first side 8b is aligned with the positioning mechanism with the time when the second side 8c is aligned with the positioning mechanism. Further, the Ori-Fla 8a of the wafer 8 as shown in FIG. 8(b) also presents the same problem. With an extremely high level of human expertise, judgements can be made visually if the maximum allowable value of the Ori-Fla linearity is $\geqq 25$ μm, if the maximum allowable linearity value of the Ori-Fla is <25 μm, there arises a problem in that it is nearly impossible to determine the measurement visually.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a linearity measuring apparatus for a wafer Ori-Fla, the linearity of which can be measured accurately in a short period of time.

The present invention provides a linearity measuring apparatus for a wafer orientation flat, comprising a base in which one, two, or more straight tracks are formed in a first direction; a platform which is configured so as to be movable in the first direction by being engaged with the straight track via engagement means, and is further provided with a top surface formed so as to be flat to

mount a wafer having an orientation flat; a block which is installed on the base with a predetermined first clearance L being provided with the straight track in a second direction perpendicular to the first direction, and has a flat face against which the orientation flat of the wafer mounted on the platform abuts and which is parallel with the first direction; wafer fixing means provided in the platform to fix the wafer in a state in which the wafer is mounted on the platform; and a measurement device which is installed on the base with a predetermined second clearance M being provided with the block in the first direction, and has a probe opposed to the straight track and capable of being displaced in the second direction, wherein when the clearance between the tip end of the probe and the straight track is taken as N, the following equation (1) is satisfied

$$0\ \mu m < L - N \leqq 100\ \mu m \quad \cdots\cdots\cdots (1)$$

In order to measure the linearity of an Ori-Fla by using the linearity measuring apparatus for a wafer Ori-Fla in accordance with the present invention, the platform on which a wafer is not mounted is first moved in the first direction so as to be opposed to the block. Next, a wafer is mounted on the top surface of the platform, and the Ori-Fla of the wafer is allowed to abut against the flat face of block so that the Ori-Fla is substantially parallel with the flat face. Thereafter, the wafer is fixed on the platform by the wafer fixing means. Next, the platform is

moved in the first direction, by which the Ori-Fla is brought into measurement range with the probe of the measurement device, the probe is then lowered to contact the Ori-Fla. Further, the platform is moved in the first direction, by which the probe of the measurement device resides on the Ori-Fla, with the probe output signal registering as deflection on the measurement device display. By reading the deflection registered on the measurement device display, the linearity of the Ori-Fla can be provided quantitatively as numerical data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of one embodiment of a linearity measuring apparatus in accordance with the present invention, showing a state before a wafer is mounted on a platform;

FIG. 2 is a plan view corresponding to FIG. 1, showing a state in which a wafer is mounted on a platform and a first Ori-Fla of the wafer is allowed to abut against a block;

FIG. 3 is a plan view corresponding to FIG. 1, showing a state in which a block is separated from a first Ori-Fla of the wafer;

FIG. 4 is a plan view corresponding to FIG. 1, showing a state in which a platform is moved together with a wafer in the first direction to bring the Ori-Fla into measurement range of the measurement device;

FIG. 5 is a sectional view taken along the line A-A of FIG. 2;

FIG. 6 is a sectional view taken along the line B-B of FIG. 3;

FIG. 7 is a sectional view taken along the line C-C of FIG. 4; and

FIG. 8 is a plan view of a wafer in which the fabrication accuracy of the Ori-Fla is poor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be described with reference to the accompanying drawings.

As shown in FIGS. 1 and 5, three straight tracks 11a such as linear motion guides (LM guides) are formed in a base 11 of a linearity measuring apparatus 10 so as to extend in a first direction, and a platform 13 engages with these straight tracks 11a via engagement means 12. This engagement means 12 has a fixed rail 14 and a movable rail 16 as shown in detail in FIG. 5. The fixed rail 14 is fixed by being inserted in the straight track 11a, and the movable rail 16 is fixed by being inserted in a groove 13a formed in the bottom surface of the platform 13 and is fitted on the fixed rail 14 via needle-shaped rollers 17. The fixed rail 14 is formed with a convex portion 14a that projects upward and extends in the longitudinal direction of the rail 14. The movable rail 16 is formed with a concave portion 16a that has a cross-sectional shape

corresponding to the convex portion 14a and a size larger than the convex portion 14a and extends in the longitudinal direction of the rail 16. The needle-shaped roller 17 is configured so as to rotatively slide on the movable rail 16 and rolls on the fixed rail 14. Thereby, the movable rail 16 is configured so as to move in the first direction along the fixed rail 14 or the straight track 11a together with the platform 13. The top surface of the platform 13 is formed so as to be flat so that a wafer 18 is mounted. The wafer 18, having a diameter in the range of 50 to 300 mm, has a first Ori-Fla 18a and a second Ori-Fla 18b. The number of straight tracks is not limited to three, and may be one, two, or more. Also, the fixed rail may be formed with a concave portion, not the convex portion, and the movable rail may be formed with a convex portion, not the concave portion. Further, between the fixed rail and the movable rail, steel balls or sliding bearings may be interposed instead of the needle-shaped rollers.

On the other hand, a block 19 is provided on the base 11 with a predetermined first clearance L (FIG. 1) being provided with the straight track 11a in a second direction perpendicular to the first direction (FIGS. 1 and 5). This block 19 is installed to the base 11 via release means 21. The block 19 is formed with a flat face 19a that is parallel with the first direction and perpendicular to the top surface of the base 11 so that the first Ori-Fla 18a or the second Ori-Fla 18b of the wafer 18 mounted on the

platform 13 can abut against the flat face 19a. The first clearance L is a clearance between the block 19 and the straight track 11a of the three straight tracks 11a which is closest to the block 19. This first clearance L is formed so as to be greater than the distance from the straight track 11a closest to the block 19 to the face of the platform 13 opposed to the block 19. As shown in detail in FIGS. 5 and 6, the release means 21 has a release body 22 installed on the base 11 behind the block 19, a rod 23 one end of which is inserted and fixed in the block 19 and the other end of which is slidably inserted in the release body 22, and an operating lever 24 the substantially central portion of which is swingingly provided on the release body 22 via a first pin 31 and the lower end of which is connected to the other end of the rod 23 via a second pin 32.

A helical compression spring 26 is provided around the rod 23. One end of this spring 26 is pressed on the block 19, and the other end thereof is pressed on the release body 22. Further, a helical tension spring 27 is provided between the release body 22 and the operating lever 24. The lower end of this spring 27 is fixed to a lower pin 28 fixed to the release body 22, and the upper end thereof is fixed to an upper pin 29 fixed to the operating lever 24. The lower pin 28 is located on the vertical line passing through the first pin 31, and the upper pin 29 is located at an upper position separated a predetermined distance

from the first pin 31 in the longitudinal direction of the operating lever 24. The operating lever 24 is configured so as to be swung between a first position (FIG. 5) at which the first Ori-Fla 18a or the second Ori-Fla 18b is allowed to abut against the flat face 19a of the block 19 and thereby the wafer 18 can be positioned and a second position (FIG. 6) at which the block 19 is separated from the first Ori-Fla 18a or the second Ori-Fla 18b, that is, the block 19 goes apart from the straight track 11a in the second direction.

The spring constant of the helical tension spring 27 is set so as to be larger than that of the helical compression spring 26. Therefore, when the operating lever 24 is operated to the second position, the elastic force of the helical tension spring 27 overcomes that of the helical compression spring 26, so that the helical tension spring 27 can temporarily hold the operating lever 24 at the second position. Reference numeral 33 in FIGS. 5 and 6 denotes a flat bar fixed to the base 11 in parallel with the straight track 11a. This flat bar 33 has a function such that when the operating lever 24 is operated to the first position (FIG. 5), the flat face 19a of the block 19 abuts against the flat bar 33, by which the flat face 19a of the block 19 is corrected so as to become parallel with the straight track 11a. Also, reference numeral 24a denotes an elongated hole formed in a lower end portion of the operating lever 24 so that the second pin 32 is

inserted in this elongated hole 24a.

On the other hand, the platform 13 is provided with wafer fixing means 34 for fixing the wafer 18 in a state in which the wafer 18 is mounted on the platform 13 (FIGS. 1 and 5). This wafer fixing means 34 includes a suction port 36 for attracting and fixing the wafer 18, which is formed in the top surface of the platform 13, a suction hole 37a one end of which communicates with the suction port 36, which is formed in the platform 13, a suction pipe 37b one end of which is connected to the other end of the suction hole 37a and the other end of which is connected to a vacuum supply (not shown), a switching valve (not shown) for switching the suction port 36 to a negative pressure or the atmospheric pressure, which is provided in the suction pipe 37b, and a selector switch 38 for turning on/off the switching valve. The suction hole 37a and the suction pipe 37b constitute a suction passage 37. The switching valve, which is an electromagnetic valve for 3-port 2-position switching, is configured so that when the selector switch 38 is turned on, the suction port 36 communicates with the vacuum supply to provide a negative pressure, and when the selector switch 38 is turned off, the suction port 36 communicates with the atmosphere to provide the atmospheric pressure. Also, a measurement device 39, for example a dial gauge having a probe 39a at the tip end of a spindle 39d is installed on the base 11 (FIGS. 1 to 4 and 7). This measurement device 39 is located on the base 11 with a

predetermined second clearance M (FIG. 1) being provided with the block 19 in the first direction, and is configured so that the probe 39a can be displaced in the second direction in such a manner as to be opposed to the straight track 11a. At the tip end of the probe 39a, there is provided a steel ball 39b capable of rolling on the first Ori-Fla 18a or the second Ori-Fla 18b. Taking a clearance between the tip end of the probe 39a and the straight track 11a as N, the measurement device 39 is fixed on the base 11 so that the following equation (1) is satisfied.

$$0\ \mu m < L - N \leqq 100\ \mu m \quad \cdots\cdots\cdots (1)$$

Preferably $40\ \mu m \leqq L - N \leqq 60\ \mu m$.

The measurement device 39 has a display 39c, for example a needle which indicates data according to displacement of the probe 39a.

A method for using an apparatus 10 for measuring the linearity of the first Ori-Fla 18a of the wafer 18, which is constructed as described above, will be described with reference to FIGS. 1 to 7.

First, the selector switch 38 is turned off, and the platform 13 on which the wafer is not mounted is moved in the first direction so that the platform 13 is opposed to the block 19. Then, the operating lever 14 is operated to the first position (FIG. 5) to cause the flat face 19a of the block 19 to abut against the flat bar 33 (FIG. 1). Next, a wafer 18 is mounted on the top surface of the platform 13, and the first Ori-Fla 18a of the wafer 18 is

caused to abut against the flat face 19a of the block 19 in such a manner as to be parallel with the flat face 19a (FIGS. 2 and 5). In this state, the selector switch 38 is turned on to cause the suction port 36 to communicate with the vacuum supply, by which the wafer 18 is attracted and fixed onto the platform 13. Next, the operating lever 24 is turned from the first position (FIG. 5) to the second position (FIG. 6) to move the block 19 in the second direction so as to be separated from the wafer 18 (FIGS. 3 and 6). In this state, the platform 13 on which the wafer 18 is mounted and fixed is moved in the first direction, by which the first Ori-Fla 18a is brought into measurement range with the tip end of the probe 39a of the measurement device 39 (FIGS. 4 and 7). When the platform 13 is further moved in the first direction, the steel ball 39b at the tip end of the probe 39a of the measurement device 39 rolls on the first Ori-Fla 18a, and a display 39c of the measurement device 39, for example a needle of the dial gauge deflects. The deflection of the display 39c of the measurement device 39 is read during rolling the steel ball 39b at the tip end of the probe 39a of the measurement device 39 from one end of the first Ori-Fla 18a to the other end thereof. The acceptability or non-acceptability of linearity of the first Ori-Fla 18a of the wafer 18 can be judged according to whether or not the deflection is within the maximum allowable value, for example, 25 μm. When the linearity of the first Ori-Fla 18a of another wafer 18 is measured

succeedingly, the selector switch 38 is turned off, and the wafer 18 having been subjected to measurement is removed from the platform 13. Thereafter, the above-described procedure is repeated. In this manner, the linearity of the first Ori-Fla 18a of the wafer 18 can be measured accurately in a short period of time.

Although the linearity of the first Ori-Fla is measured by using the linearity measuring apparatus in the above-described embodiment, the linearity of the second Ori-Fla may also be measured by the same sequential method.

Furthermore, in the above-described embodiment, the deflection registered on the measurement device display is read visually. However, if the linearity measuring apparatus is configured so that the deflection data of the measurement device display can be outputted as an electronic signal, the Ori-Fla linearity data for each wafer can be stored by connecting the electronic signal to the input of a computer, and also the acceptability or non-acceptability of the linearity of the Ori-Fla can be analyzed/determined by means of the computer when the apparatus of the present invention is automated.

The present invention achieves the following effects: as described above, according to the present invention, the platform is moved in the first direction so as to be opposed to the block, a wafer is fixed on the platform so that the Ori-Fla abuts against the block, the block is retracted, and the platform is moved in the first direction

so that the Ori-Fla is brought into measurement range with the probe of the measurement device, and the probe is lowered until contact with the Ori-Fla is made. Therefore, by reading the deflection of the display of the measurement device when the Ori-Fla is moved from one end to the other end thereof, the linearity of the Ori-Fla can be displayed quantitatively as numerical data so that the acceptability or non-acceptability of linearity of the Ori-Fla of the wafer can be determined. As a result, the linearity of the Ori-Fla of the wafer can be measured accurately in a short period of time.

Also, if the wafer fixing means has the suction port for attracting and fixing the wafer, the suction passage communicating with the suction port, and the switching valve for switching the suction port to a negative pressure or the atmospheric pressure, the wafer can be fixed on the platform by a very simple operation without damage to the wafer.

Also, if the release means for moving the block in the second direction in which the block retracts from the straight track is provided, the Ori-Fla moves in a state of being separated from the block when the platform with the wafer being mounted thereon is moved in the first direction. As a result, the wafer is not damaged.

Further, if the linearity measuring apparatus is configured so that the deflection data of the measurement device display can be outputted as an electronic signal,

the Ori-Fla linearity data for each wafer can be stored by connecting the electronic signal to the input of a computer, and also the acceptability or non-acceptability of linearity of the Ori-Fla can be analyzed/determined by means of the computer when the apparatus of the present invention is automated.

EXHIBIT 7

WHAT IS CLAIMED IS:

1. A linearity measuring apparatus for a wafer orientation flat, comprising:

a base in which one, two, or more straight tracks are formed in a first direction;

a platform which is configured so as to be movable in said first direction by being engaged with said straight track via engagement means, and is further provided with a top surface formed so as to be flat to mount a wafer having an orientation flat;

a block which is installed on said base with a predetermined first clearance L being provided with the straight track in a second direction perpendicular to said first direction, and has a flat face against which the orientation flat of said wafer mounted on said platform abuts and which is parallel with said first direction;

wafer fixing means provided in said platform to fix said wafer in a state in which said wafer is mounted on said platform; and

a measurement device which is installed on said base with a predetermined second clearance M being provided with said block in said first direction, and has a probe opposed to said straight track and capable of being displaced in said second direction, wherein

when a clearance between the tip end of said probe and said straight track is taken as N, the following equation (1) is satisfied

$0\ \mu m < L - N \leqq 100\ \mu m$ ····· (1)

2. The linearity measuring apparatus according to claim 1, wherein said wafer fixing means has a suction port formed in said platform to attract and fix said wafer, a suction passage communicating with said suction port, and a switching valve provided in said suction passage to switch said suction port to a negative pressure or the atmospheric pressure.

3. The linearity measuring apparatus according to claim 1, wherein release means for moving said block in said second direction in which said block goes apart from said straight track is installed on said base.

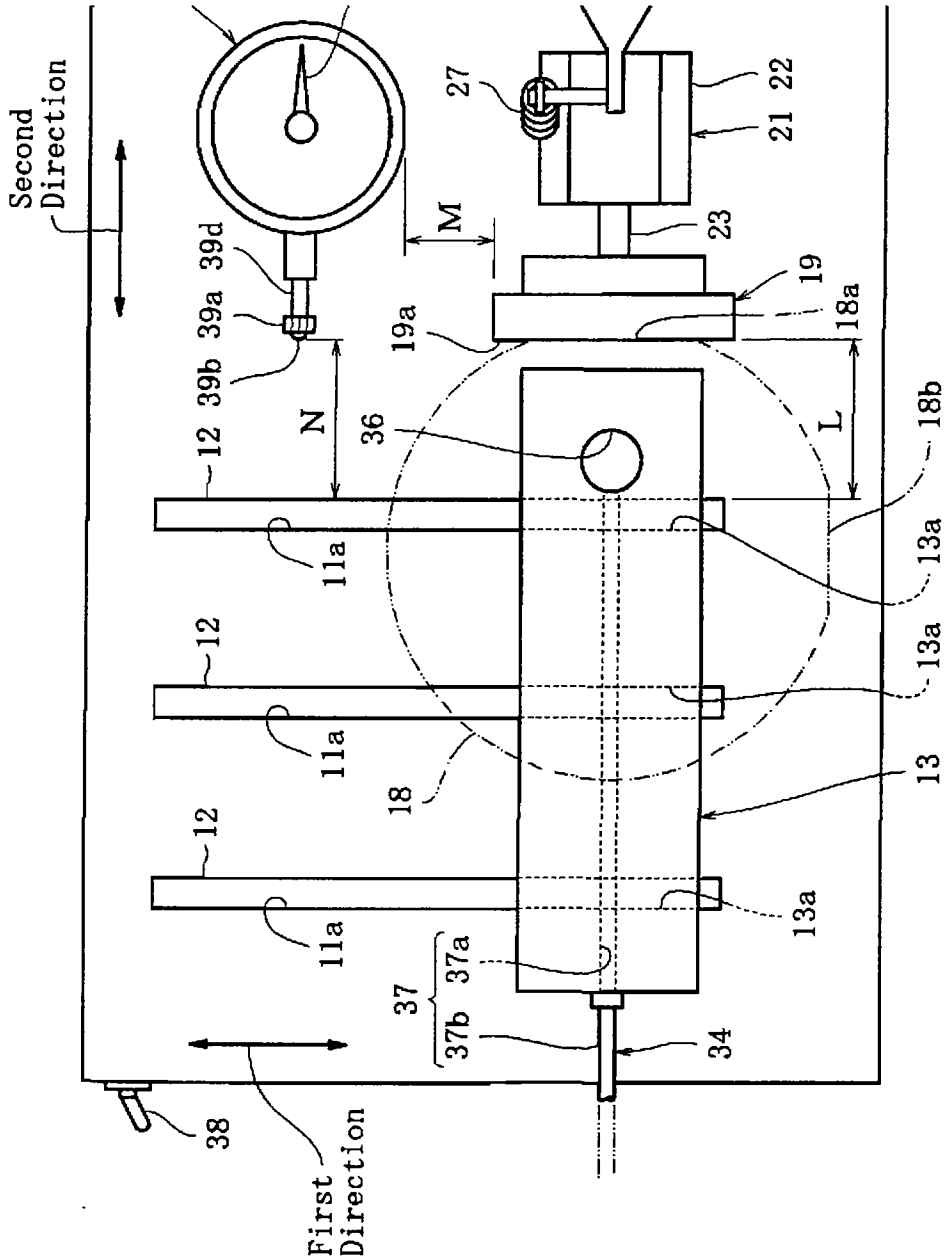
4. The linearity measuring apparatus according to claim 1, wherein deflection data displayed on said measurement device can be outputted as an electronic signal.

5. The linearity measuring apparatus according to claim 1, wherein said apparatus can be applied to a wafer having a diameter in the range of 50 to 300 mm.

EXHIBIT 7

ABSTRACT OF THE DISCLOSURE

Straight tracks are formed in a first direction on a base. The top surface of a platform is formed so as to be flat to mount a wafer having an Ori-Fla, and the platform is moved in the first direction by being engaged with the straight tracks via engagement means. A block having a flat face against which the Ori-Fla of the wafer abuts and which is parallel with the first direction is installed with a first clearance L being provided with the straight track in a second direction perpendicular to the first direction. Wafer fixing means for fixing the wafer in a state in which the wafer is mounted on the platform is provided in the platform, and a measurement device having a probe opposed to the straight track and capable of being displaced in the second direction is installed on the base with a second clearance M being provided with the block in the first direction. When a clearance between the tip end of the probe and the straight track is taken as N, the relationship of $0\ \mu m < L-N \leqq 100\ \mu m$ exists. By this configuration, the linearity of the Ori-Fla can be measured accurately in a short period of time.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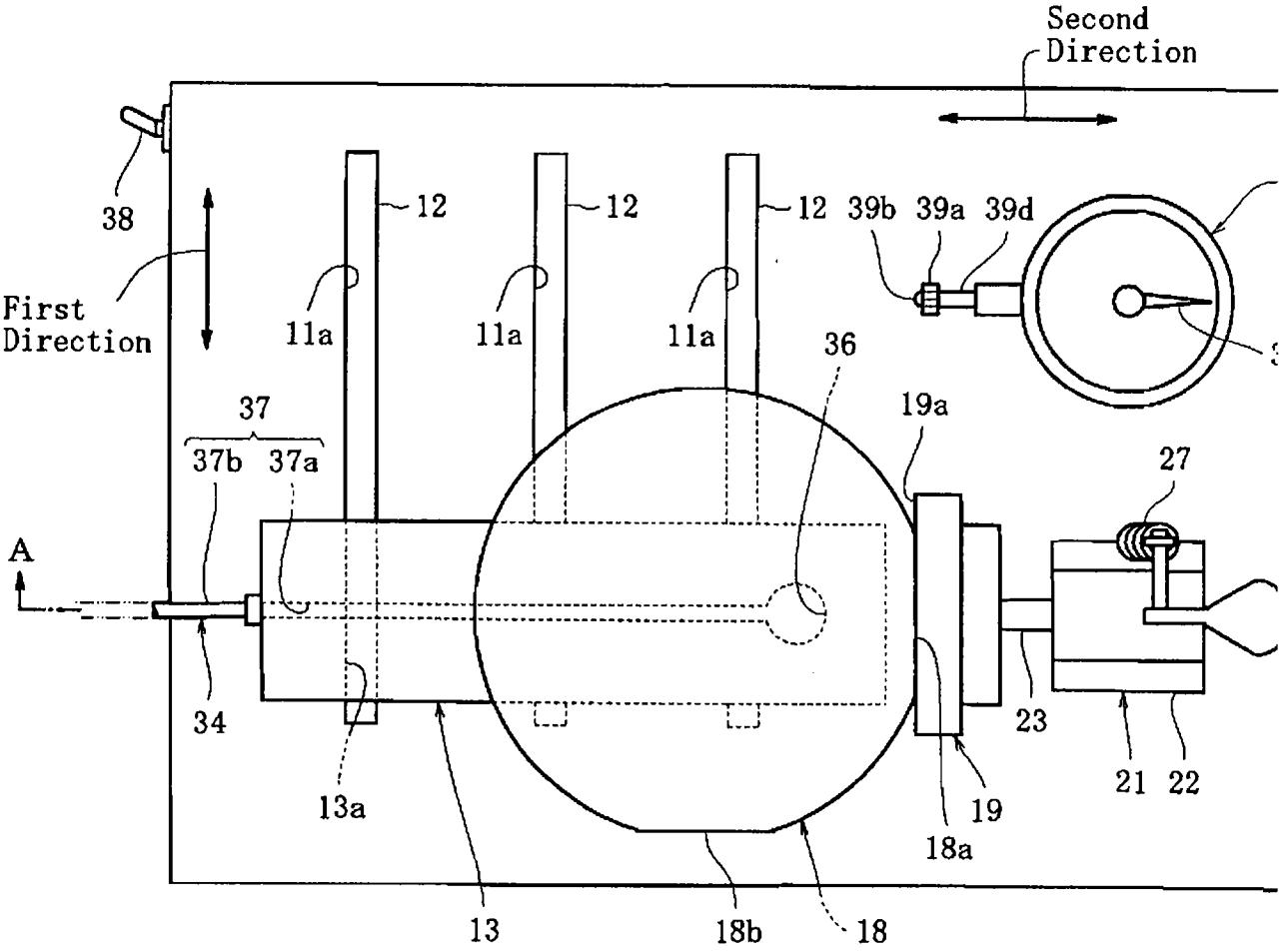
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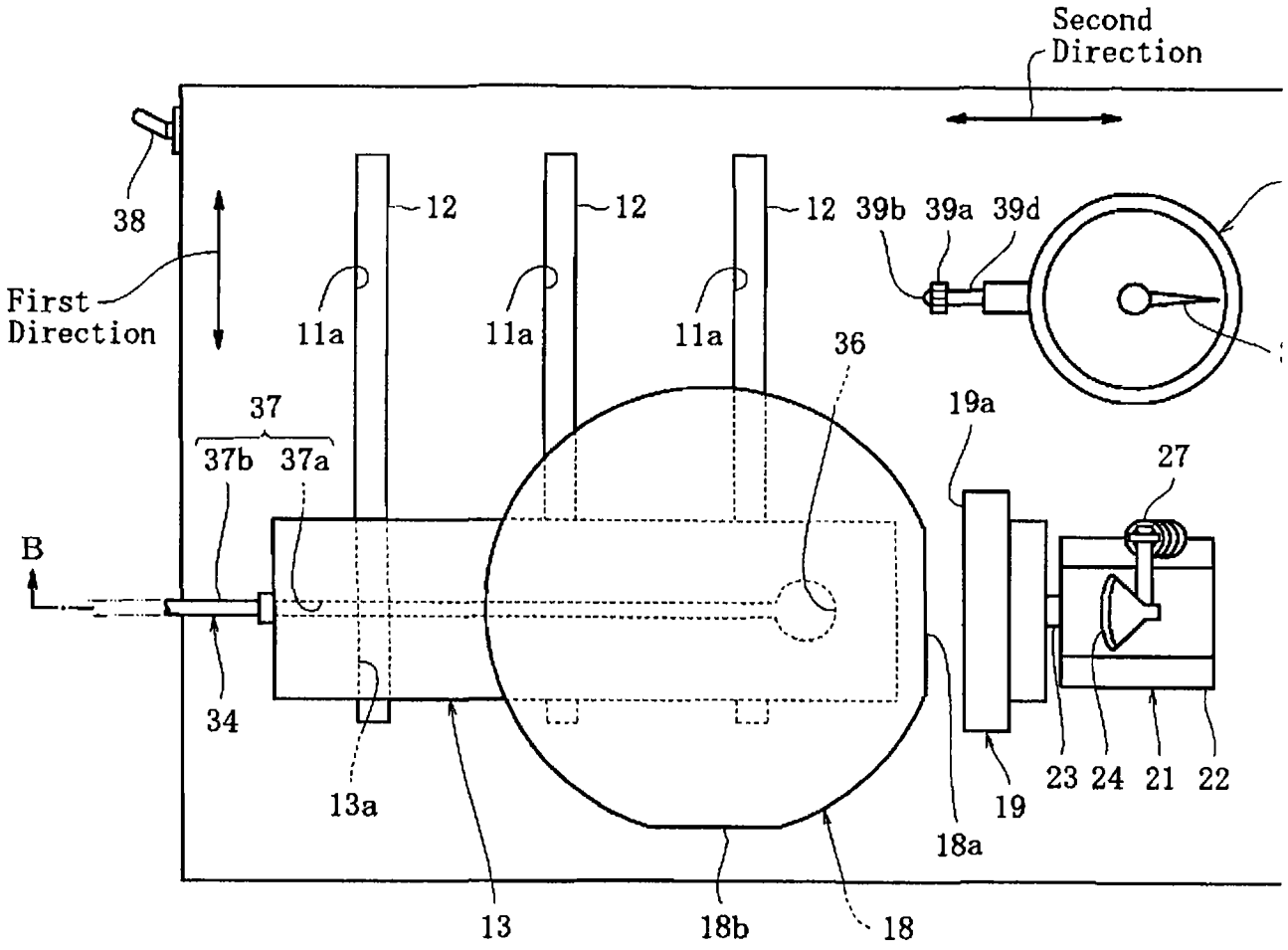
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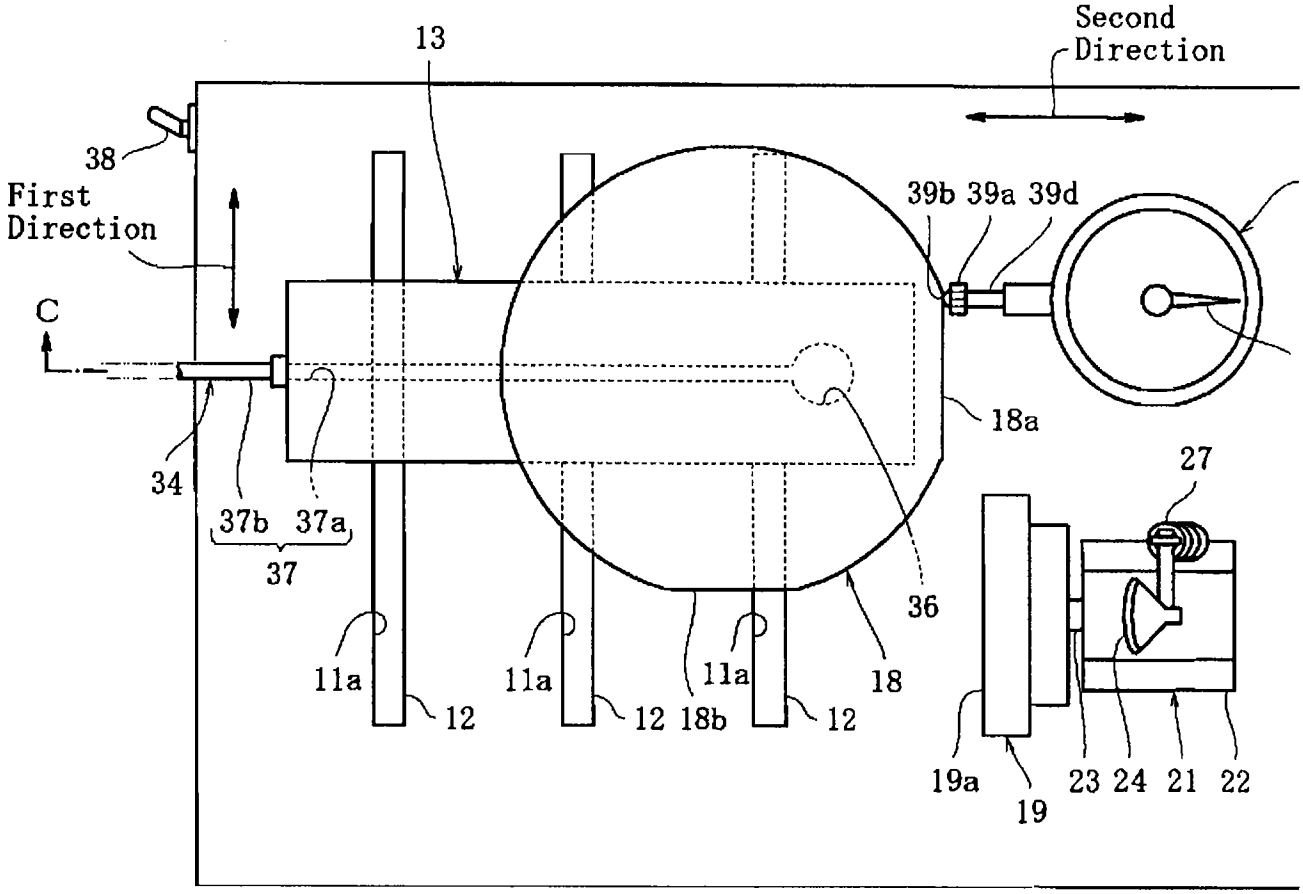
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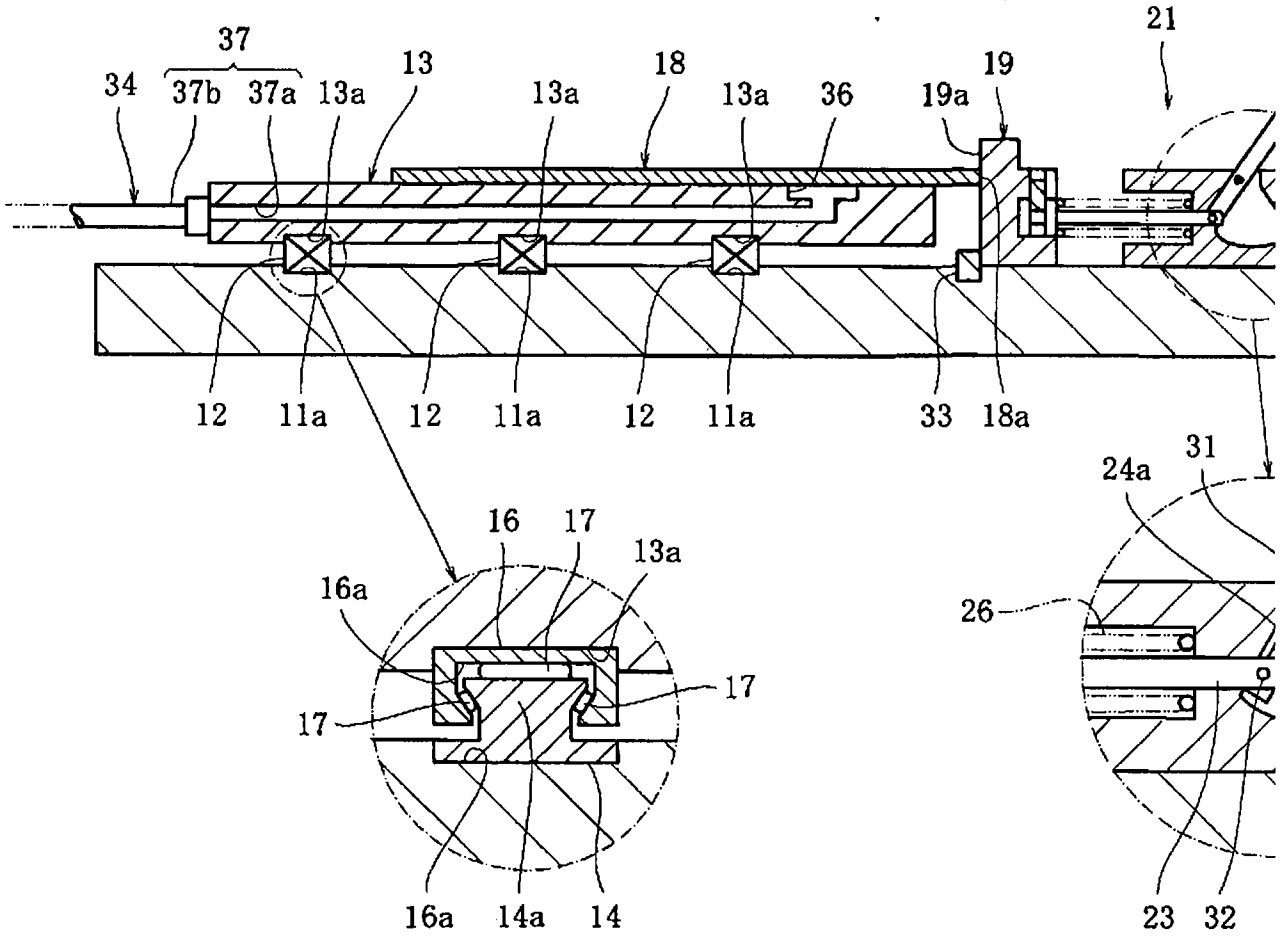
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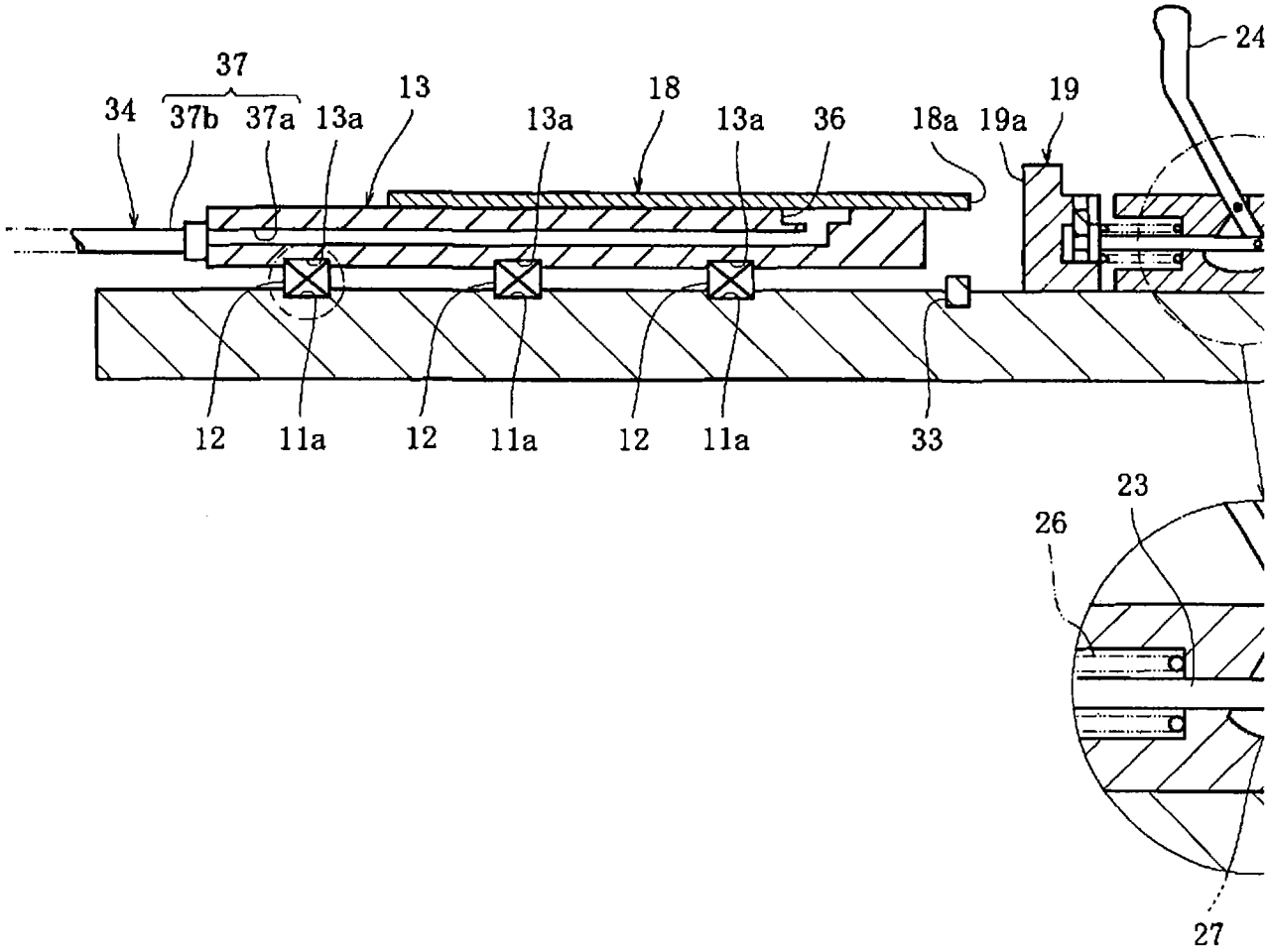
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Fig. 7

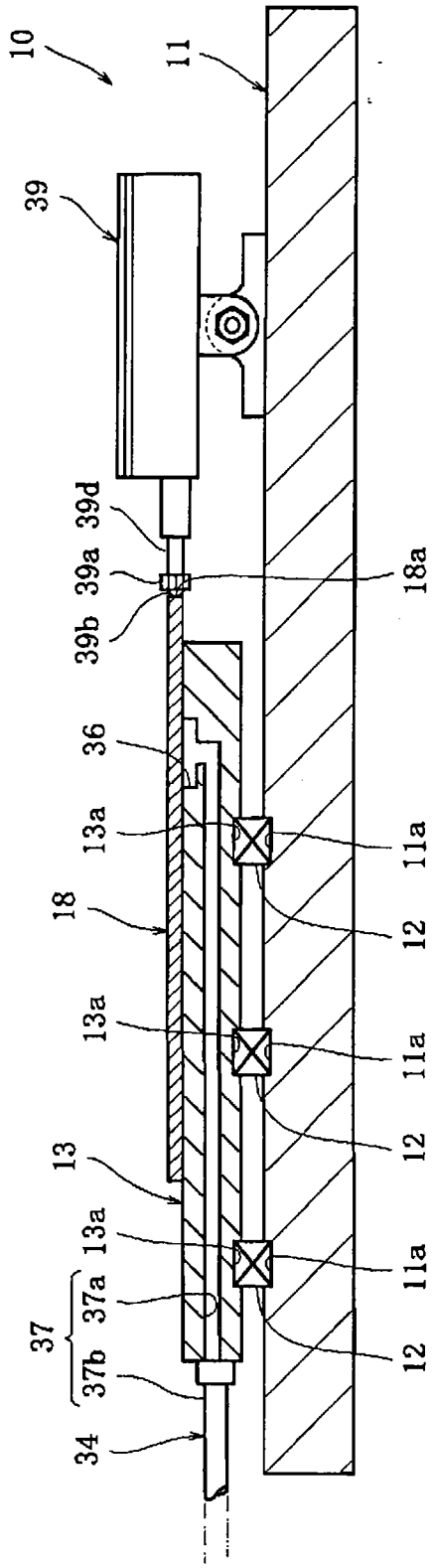
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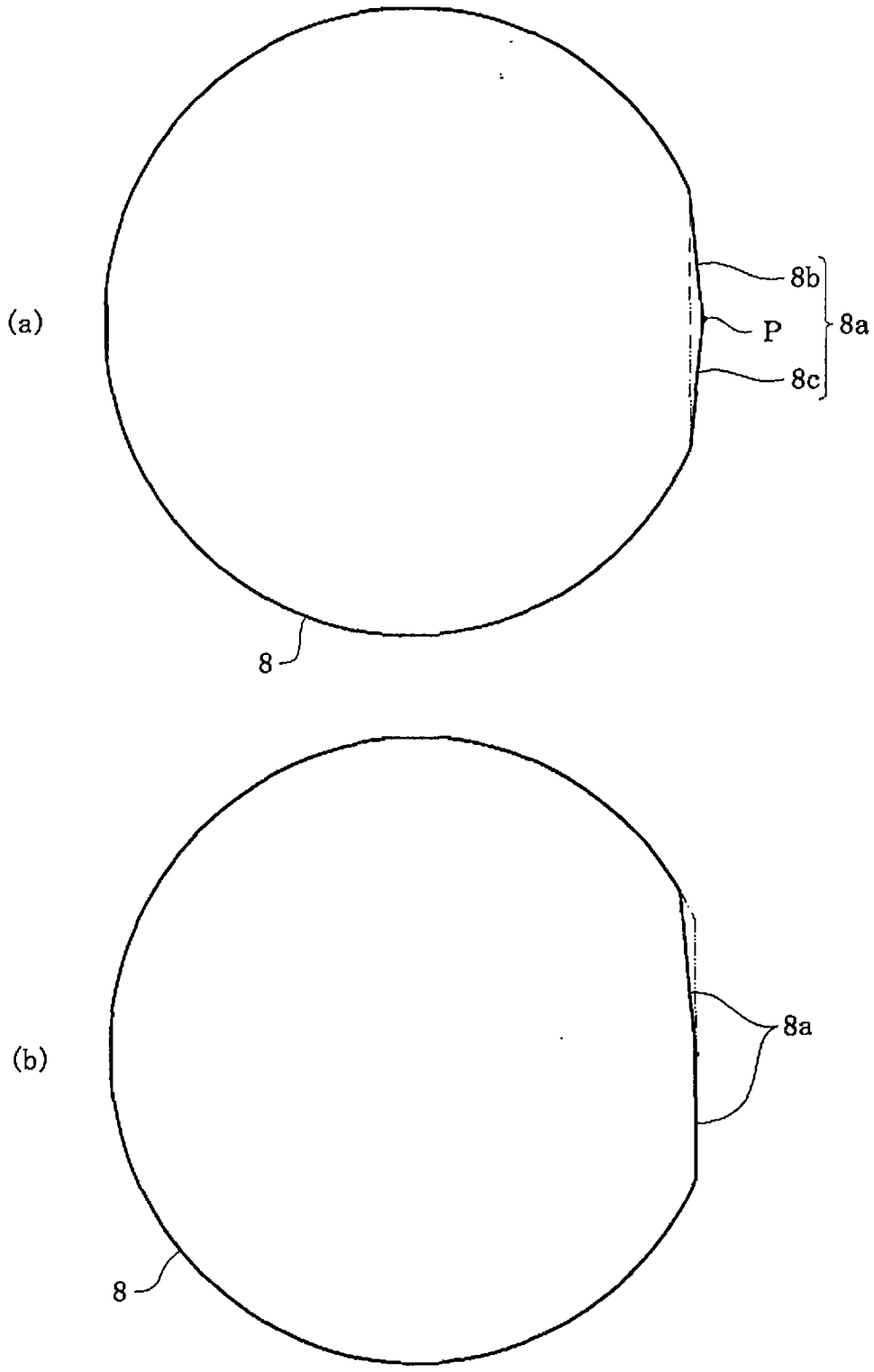
Fig. 8



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SERIAL NUMBER	REQUEST DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
P-104,253	5/31/01	CINDY KOHANEK, ET AL	JG-SU-5072

Title: **LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT**

Art Unit	Paper Number

Correspondence Address:
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EXHIBIT 7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Cindy Kohanek and Gary Babb** Serial No.: not yet filed Atty. Docket No.: JG-SU-5072	PRIMARY FLAT LINEARITY GAUGE

New York, NY 10152

PETITION FOR EXPEDITED ISSUANCE OF FOREIGN FILING LICENSE PURSUANT TO 37 CFR SEC. 5.12 AND 5.13

Asst. Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicants respectfully request that a foreign filing license be issued covering the subject matter of the attached disclosure, and that such request be handled in an expedited manner.

Enclosed please find payment of $130.00, the statutory fee. Please charge any additional fees to Deposit Account No. 50-15290.

Respectfully submitted,

Dated: May 30, 2001

Jules E. Goldberg
Reg. No. 24,408

REED SMITH LLP
375 Park Avenue, 17th Fl.
New York, NY 10152
(212) 521-5403

Attorney for Applicant

LINEARITY MEASURING APPARATUS FOR WAFER ORIENTATION FLAT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a measuring apparatus that provides numerical data relative to the linearity of an orientation flat (hereinafter referred to as an Ori-Fla).

Description of Related Art

Conventionally, examination of the linearity of an Ori-Fla portion has been by visual methodology, with no provision of quantitative data in which to make judgements. On the other hand, there has been disclosed a wafer Ori-Fla positioning method in which an Ori-Fla is positioned by pressing a wafer against a positioning mechanism provided on a wafer chuck mounting surface (Unexamined Japanese Patent Publication No. 10-22368). In this positioning method, the wafer chuck mounting surface is provided so as to be inclined, and a gas flow for floating a wafer with respect to a wafer chuck is generated by air blowing means.

In the positioning method configured as described above, when air is blown from the air blowing means in a state in which a wafer is mounted on the wafer chuck mounting surface, the wafer moves smoothly under gravity toward a positioning mechanism along the inclination of the wafer chuck mounting surface. As a result, the positioning of Ori-Fla can be performed reliably.

Further, there has been disclosed an exposure device that has a stage, a rough positioning mechanism, and number detecting means, and can perform exact rough positioning of a wafer without pattern at the time of first-level pattern exposure (Unexamined Japanese Patent Publication No. 8-78316). In this exposure device, at least three stopper members are provided to roughly position a wafer on the stage, and the stage moves in the longitudinal and transverse X & Y directions and in the rotation direction of θ. Also, the rough positioning mechanism performs rough positioning by causing the peripheral portions of wafer mounted on the stage to abut against the stopper members. Further, the number detecting means detects an identification number scribed on the wafer positioned roughly so that the wafer moves on the stage until the identification number arrives at a predetermined position.

In the conventional method in which the linearity of

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Ori-Fla portion is examined visually, however, the acceptability or non-acceptability of linearity cannot be determined quantitatively. Also, in the conventional Ori-Fla positioning method disclosed in the aforementioned Unexamined Japanese Patent Publication No. 10-22368, or in the exposure device disclosed in Unexamined Japanese Patent Publication No. 8-78316, the fabrication accuracy of Ori-Fla, especially the fabrication accuracy in chamfering Ori-Fla is poor because the linearity of the Ori-Fla of **the wafer itself** is not measured. For example, when as shown in FIG. 8(a), a vertex P is formed at the center of an Ori-Fla 8a, and the Ori-Fla 8a is formed of a first side 8b and a second side 8c on opposite sides of the vertex P, there arises a problem in that the crystalline orientation of a wafer 8 deflects comparing the time when the first side 8b is aligned with the positioning mechanism with the time when the second side 8c is aligned with the positioning mechanism. Further, the Ori-Fla 8a of the wafer 8 as shown in FIG. 8(b) also presents the same problem. **With an extremely high level of human expertise, judgements can be made visually if the maximum allowable value of the Ori-Fla linearity is ≥25μm, if the maximum allowable linearity value of the Ori-Fla is <25μm, there arises a problem in that it is nearly impossible to determine the measurement visually.**

SUMMARY OF THE INVENTION

The present invention has been made to solve the above problems **by providing a method of accurately measuring the linearity of the Ori-Fla of a wafer in a short period of time.**

A first mode of the present invention provides a linearity measuring apparatus for a wafer orientation flat, comprising a base in which **one, two, or more** straight tracks are formed in a first direction; a platform which is configured so as to be movable in the first direction by being engaged with the straight track via engagement means, and is further provided with a top surface formed so as to be flat to mount a wafer having an orientation flat; a block which is installed on the base with a predetermined first clearance L being provided with the straight track in a second direction perpendicular to the first direction, and has a flat face against which the orientation flat of the wafer mounted on the platform abuts and which is parallel with the first direction; wafer fixing means provided in the platform to fix the wafer in a state in which the wafer is mounted on the platform; and a **measurement device*** which is installed on the base with a predetermined clearance M being provided with the block in